LD6935 series

Dual low-dropout regulators, high PSRR, 300 mA

Rev. 1 — 29 May 2013 Preliminary data sheet

1. Product profile

1.1 General description

The LD6935 series consists of small-size dual Low DropOut regulators (LDO). Each device delivers two times 300 mA with a typical voltage drop of 240 mV at 300 mA for each LDO. Each device offers two individual fixed nominal output voltages ($V_{O(nom)}$) from 1.2 V to 3.6 V.

The LDO has an integrated Soft start to control the inrush current during start-up. The output states when disabled can be high-ohmic 3-state or auto discharge. Optionally a delayed output circuit is available for the second output. The devices are available in DFN1612-8 (SOT1225) plastic package with a height of 0.4 mm.

1.2 Features and benefits

- Extremely low standby current in shutdown mode ($\leq$ 0.1 μA)
- Low quiescent current
- Low output noise
- Fast turn-on time
- High Power Supply Rejection Ratio (PSRR)
- Auto discharge or high-ohmic mode for output states when disabled
- Delayed output circuit for second LDO (optional)
- DFN1612-8 (SOT1225) leadless package 1.6 × 1.2 × 0.4 mm
- Pb-free, Restriction of Hazardous Substances (RoHS) compliant, free of halogen and antimony (Dark Green compliant)

1.3 Applications

- Smartphones
- Mobile handsets
- Digital still cameras
- Tablet PCs
- Mobile internet devices
- Portable media players

1.4 Quick reference data

- I_O = 300 mA for each LDO
- PSRR = 80 dB at 1 kHz
- RMS noise $V_{n(o)RMS}$ = 60 μV at 10 Hz to 100 kHz
- $t_{startup(reg)}$ = 150 μs
- V_I = 1.75 V to 5.5 V
- V_O = 1.2 V to 3.6 V (fixed value)
- Dropout voltage V_{do} = 240 mV at I_O = 300 mA for each LDO
- Quiescent current I_q = 2 × 35 μA at I_O = 0 mA

2. Pinning information

2.1 Pinning

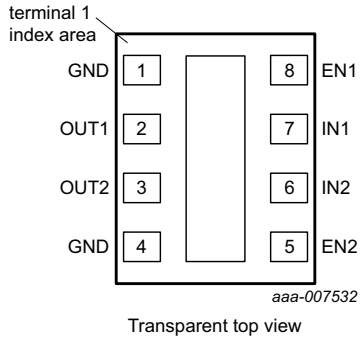


Fig 1. Pin configuration for DFN1612-8 (SOT1225)

2.2 Pin description

Table 1. Pin description for DFN1612-8 (SOT1225)

Symbol	Pin	Description
GND	1	supply ground
OUT1	2	regulator 1 output voltage
OUT2	3	regulator 2 output voltage
GND	4	supply ground
EN2	5	regulator 2 enable input
IN2	6	regulator 2 supply voltage input
IN1	7	regulator 1 supply voltage input
EN1	8	regulator 1 enable input
i.c.	TAB	internal connected [1]

[1] The TAB is GND level (it is placed on the reverse side of the IC).
It is recommended to connect the TAB to GND. Leaving it unconnected is also allowed but it may result in lower thermal performance.

3. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
LD6935L	DFN1612-8	plastic extremely thin small outline package; no leads; 8 terminals; body 1.6 × 1.2 × 0.4 mm	SOT1225

3.1 Ordering options

Further output voltage information available on request; see Section 19 “Contact information”.

Table 3. Type number and nominal output voltage of high-ohmic output

Type number	Nominal output voltage $V_{O(nom)}$	
	OUT1	OUT2
LD6935L/2828H	2.8 V	2.8 V
LD6935L/3318H	3.3 V	1.8 V

Table 4. Type number and nominal output voltage of pull-down output

Type number	Nominal output voltage $V_{O(nom)}$	
	OUT1	OUT2
LD6935L/1828P	1.8 V	2.8 V
LD6935L/2828P	2.8 V	2.8 V
LD6935L/3318P	3.3 V	1.8 V
LD6935L/3328P	3.3 V	2.8 V
LD6935L/3333P	3.3 V	3.3 V

Table 5. Type number and nominal output voltage of pull-down output with delay circuit

Type number	Nominal output voltage $V_{O(nom)}$	
	OUT1	OUT2
LD6935L/3118PD	3.1 V	1.8 V

4. Block diagram

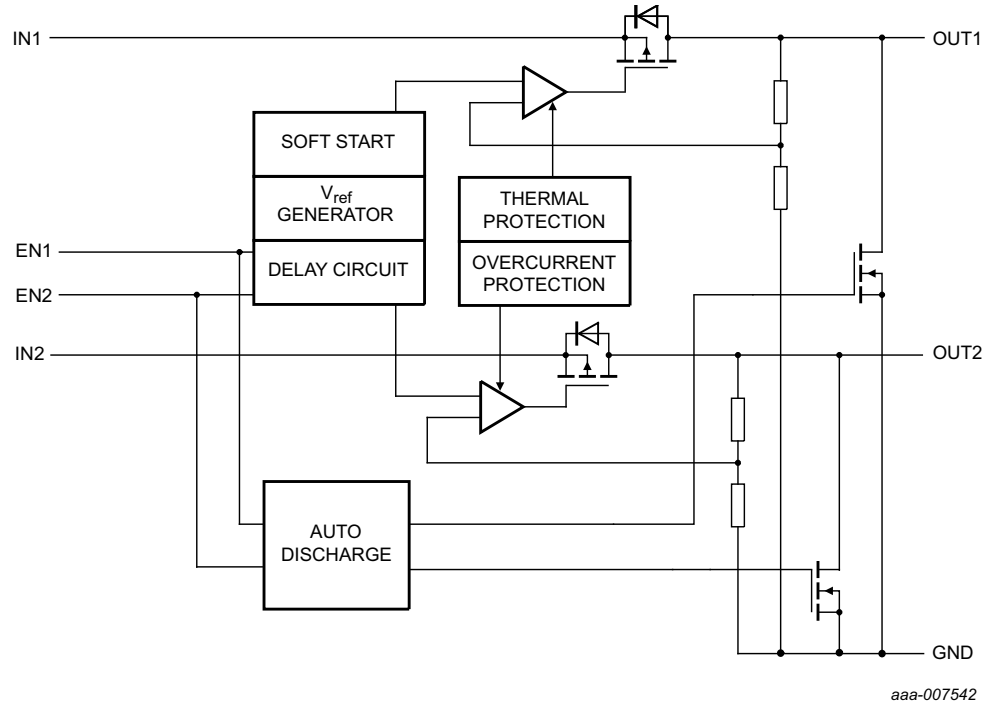


Fig 2. Block diagram dual LDO with auto discharge function (-P and -PD versions)

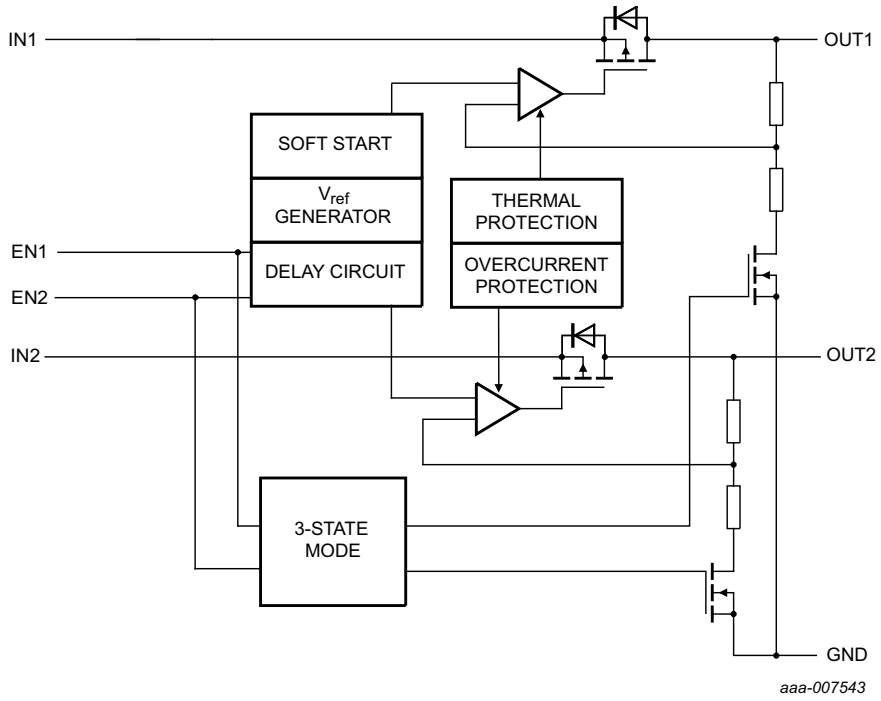


Fig 3. Block diagram dual LDO with high-ohmic output (-H version)

5. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
Pin IN1, IN2, EN1 and EN2						
V_I	input voltage	4 ms transient		−0.5	+6.0	V
V_{EN}	voltage on pin EN	4 ms transient		−0.5	+6.0	V
Pin OUT1 and OUT2						
V_O	output voltage	4 ms transient		−0.5	+6.0	V
P_{tot}	total power dissipation		[1]	-	740	mW
T_{stg}	storage temperature			−55	+150	°C
T_j	junction temperature			−40	+125	°C
T_{amb}	ambient temperature			−40	+85	°C
V_{ESD}	electrostatic discharge voltage	human body model	[2]	-	±2	kV
		machine model	[3]	-	±200	V

[1] The (absolute) maximum power dissipation depends on the junction temperature T_j. Higher power dissipation is allowed with lower ambient temperatures. The conditions to determine the specified values are T_{amb} = 25 °C and the use of a two-layer Printed-Circuit Board (PCB).

[2] According to JESD22-A114F.

[3] According to JESD22-A115C.

6. Recommended operating conditions

Table 7. Operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
T_{amb}	ambient temperature			−40	+85	°C
T_j	junction temperature			-	+125	°C
Pin IN1 and IN2						
V_I	input voltage			1.75	5.5	V
$C_{ext(IN)}$	external capacitance on pin IN		[1]	1.0	-	µF
Pin EN1 and EN2						
V_{EN}	voltage on pin EN			0	V_I	V
Pin OUT1 and OUT2						
V_O	output voltage			0	V_I + 0.3	V
$C_{L(ext)}$	external load capacitance			1.0	-	µF

[1] See Section 10.1 “Input and output capacitor values”.

7. Thermal characteristics

Table 8. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1][2]	135	K/W

[1] The overall $R_{th(j-a)}$ can vary depending on the board layout. To minimize the effective $R_{th(j-a)}$, all pins must have a solid connection to larger Cu layer areas for example to the power and ground layer. In multilayer PCB applications, use the second layer to create a large heat spreader area directly below the LDO. If this layer is either ground or power, connect it with several vias to the top layer connecting to the device ground or supply. Avoid using solder-stop varnish under the chip.

[2] Use the measurement data given for a rough estimation of the $R_{th(j-a)}$ in your application. The actual $R_{th(j-a)}$ value can vary in applications using different layer stacks and layouts.

8. Characteristics

Table 9. Electrical characteristics

At recommended input voltages and T_{amb} = −40 °C to +85 °C; voltages are referenced to GND (ground = 0 V); unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Output voltage per LDO							
V_{do}	dropout voltage	I_O = 300 mA; $V_I \leq V_{O(nom)}$	[2]	-	240	-	mV
ΔV_O	output voltage variation	$V_O \geq$ 1.8 V; I_O = 1 mA					
		T_{amb} = +25 °C		-2	-	+2	%
		−30 °C ≤ T_{amb} ≤ +85 °C	[2]	-3	-	+3	%
		V_O < 1.8 V; I_O = 1 mA					
		T_{amb} = +25 °C		−3	-	+3	%
		−30 °C ≤ T_{amb} ≤ +85 °C	[2]	−4	-	+4	%
Line regulation error per LDO							
$\Delta V_O/(V_O x \Delta V_I)$	relative output voltage variation with input voltage	$V_I = (V_{O(nom)} + 1\ V)$ to 5 V; I_O = 1 mA	[2]	−0.1	-	+0.1	%/V
Load regulation error per LDO							
$\Delta V_O/(V_O x \Delta I_O)$	relative output voltage variation with output current	1 mA ≤ I_{OUT} ≤ 300 mA; $V_I = (V_{O(nom)} + 1\ V)$	[2]	-0.01	±0.0025	0.01	%/mA
Output current per LDO							
I_O	output current		[2]	300	-	-	mA
$I_{act(fold)}$	foldback activation current		[2]	-	750	-	mA
I_{sc}	short-circuit current	V_O = 0 V	[2]	-	100	-	mA
Regulator input current per LDO							
$I_{inrush(lim)}$	inrush current limit	$C_{L(ext)}$ = 1 µF at OUT1 and OUT2	[2]	-	-	400	mA
I_q	quiescent current	(V_{EN1} or V_{EN2}) > 1.1 V; I_O = 0 mA at OUT1 and OUT2; $V_I = (V_{O(nom)} + 1\ V)$		-	35	50	µA
		(V_{EN1} or V_{EN2}) > 1.1 V; 1 mA ≤ I_O ≤ 300 mA at OUT1 and OUT2; $V_I = (V_{O(nom)} + 1\ V)$	[2]	-	400	-	µA
		(V_{EN1} or V_{EN2}) ≤ 0.4 V		-	0.1	1.0	µA

Table 9. Electrical characteristics *...continued*

At recommended input voltages and T_{amb} = −40 °C to +85 °C; voltages are referenced to GND (ground = 0 V); unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Ripple rejection and output noise per LDO							
PSRR	power supply rejection ratio	$V_I = V_{O(nom)} + 1$ V; I_O = 30 mA; f_{ripple} = 1 kHz	[2]	-	80	-	dB
$V_{n(o)(RMS)}$	RMS output noise voltage	bandwidth = 10 Hz to 100 kHz; $C_{L(ext)}$ = 1 µF; V_O = 1.8 V	[2]	-	60	-	µV
Enable input and timing (pin EN1, pin EN2) per LDO							
V_{IL}	LOW-level input voltage			0	-	0.4	V
V_{IH}	HIGH-level input voltage			1.1	-	5.5	V
I_{en}	enable current			-	400	-	nA
$t_{startup(reg)}$	regulator start-up time	for each LDO; V_I = 5.5 V; $V_O = 0.95 \times V_{O(nom)}$; I_O = 300 mA; $C_{L(ext)}$ = 1 µF	[2]	-	150	-	µs
t_d	delay time	for LDO2; -PD version	[2]	-	100	-	µs
Automatic discharge function (LD6935L/xxxxP or LD6935L/xxxxPD) per LDO							
R_{pd}	pull-down resistance		[2]	-	100	-	Ω
$t_{sd(reg)}$	regulator shutdown time	V_I = 5.5 V; $C_{L(ext)}$ = 1 µF; I_O = 0 A; $V_O = 0.1 \times V_{O(nom)}$	[2]	-	300	-	µs
Thermal protection							
T_{sd}	shutdown temperature		[2]	-	160	-	°C
$T_{sd(hys)}$	shutdown temperature hysteresis		[1][2]	-	20	-	°K

[1] The junction temperature must decrease by $T_{sd(hys)}$ to enable the device after T_{sd} was reached and the device was disabled.

[2] The parameter was verified and is guaranteed by design.

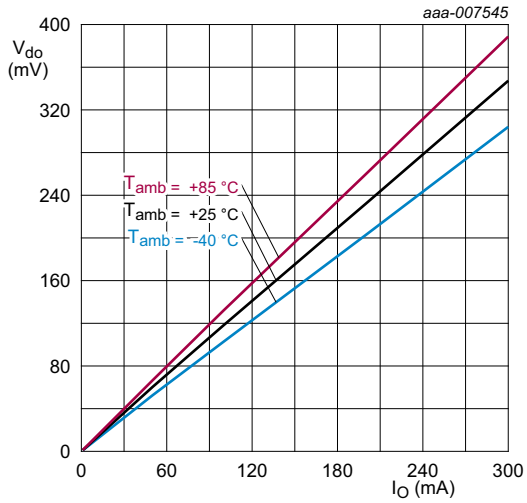
9. Dynamic behavior

All results described in Section 9 are based on measurements of types LD6935L/xxxxH from the LD6935 product series.

9.1 Dropout

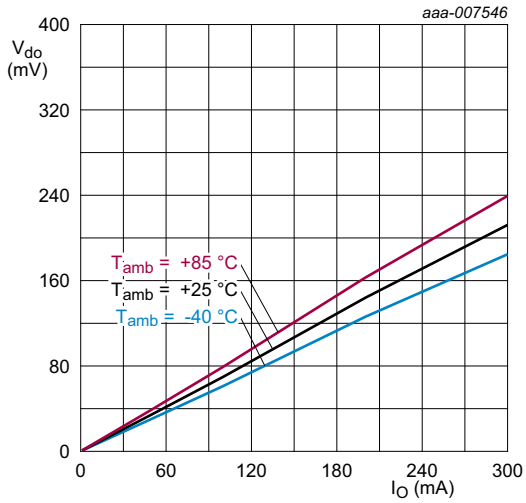
The dropout voltage is defined as the smallest input-to-output voltage difference at a specified load current when the regulator operates within its linear region with the pass transistor functioning simply as a resistor. This means that the input voltage is below the nominal output voltage value.

A small dropout voltage guarantees lower power consumption and maximizes efficiency.



V_I = 1.7 V; $V_{O(nom)}$ = 1.8 V; $C_{L(ext)}$ = 1 µF; $C_{ext(IN)}$ = 1 µF

Fig 4. Dropout voltage as a function of output current for LD6935L/3318x

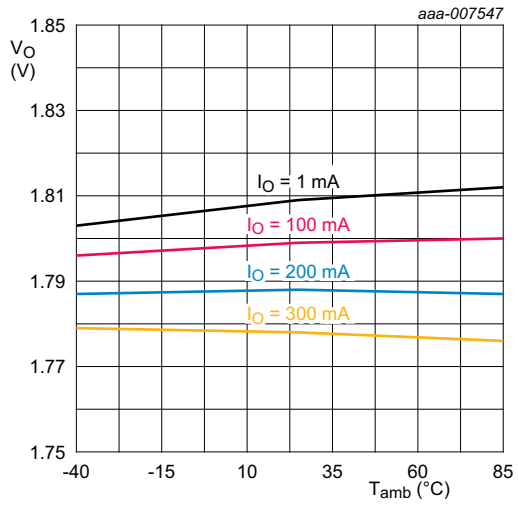


V_I = 3.2 V; $V_{O(nom)}$ = 3.3 V; $C_{L(ext)}$ = 1 µF; $C_{ext(IN)}$ = 1 µF

Fig 5. Dropout voltage as a function of output current for LD6935L/3318x

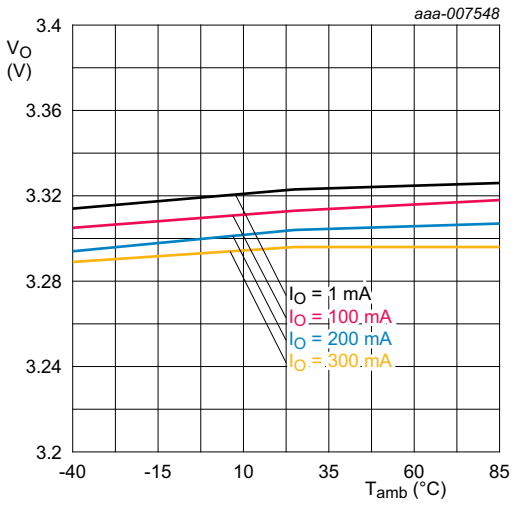
9.2 Working voltage tolerance

The guaranteed output voltages are specified in Table 9.



V_I = 4.5 V; $V_{O(nom)}$ = 1.8 V; $C_{L(ext)}$ = 1 µF; $C_{ext(IN)}$ = 1 µF

Fig 6. Working voltage tolerance for LD6935L/3318x

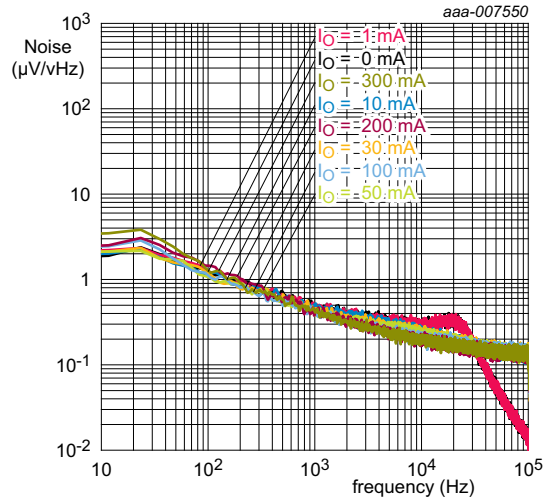


V_I = 4.5 V; $V_{O(nom)}$ = 3.3 V; $C_{L(ext)}$ = 1 µF; $C_{ext(IN)}$ = 1 µF

Fig 7. Working voltage tolerance for LD6935L/3318x

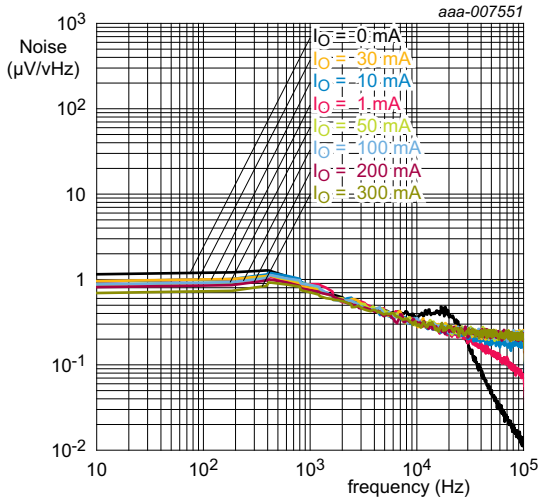
9.3 Noise

Output noise voltage of an LDO circuit is given as noise density or RMS output noise voltage over a defined range of frequencies (10 Hz to 100 kHz). Permanent conditions are a constant output current and a ripple-free input voltage. The output noise voltage is generated by the LDO regulator.



V_I = 4.5 V; $V_{O(nom)}$ = 1.8 V; $C_{L(ext)}$ = 1 µF; $C_{ext(IN)}$ = 1 µF

Fig 8. Noise density for LD6935L/3318x

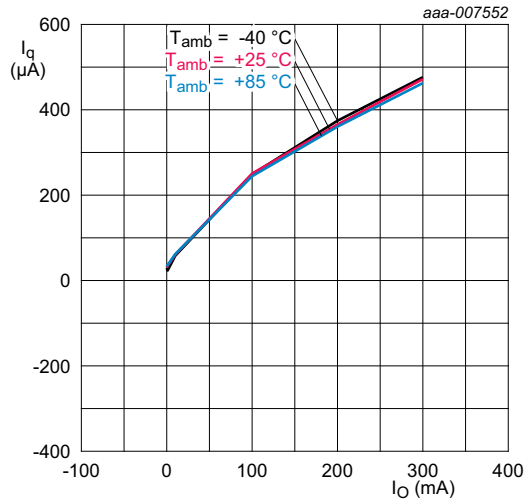


V_I = 4.5 V; $V_{O(nom)}$ = 3.3 V; $C_{L(ext)}$ = 1 µF; $C_{ext(IN)}$ = 1 µF

Fig 9. Noise density for LD6935L/3318x

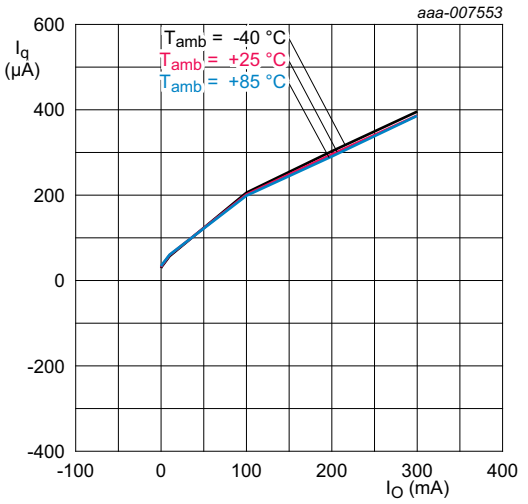
9.4 Quiescent current

Quiescent or ground current is the difference between the input and the output current of the regulator.



V_I = 4.5 V; $V_{O(nom)}$ = 1.8 V; $C_{L(ext)}$ = 1 μF; $C_{ext(IN)}$ = 1 μF

Fig 10. Quiescent current for LD6935L/3318x



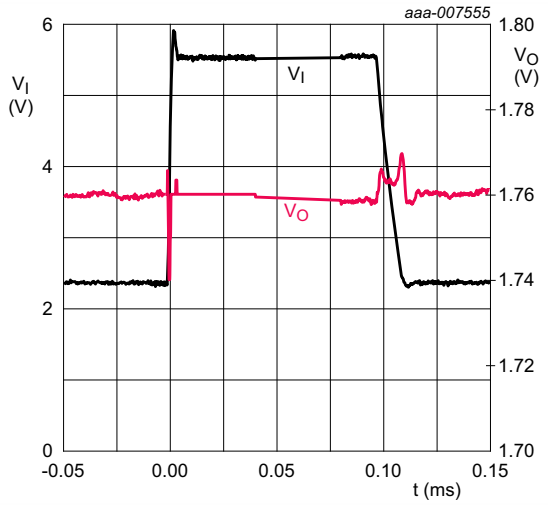
V_I = 4.5 V; $V_{O(nom)}$ = 3.3 V; $C_{L(ext)}$ = 1 μF; $C_{ext(IN)}$ = 1 μF

Fig 11. Quiescent current for LD6935L/3318x

9.5 Line regulation

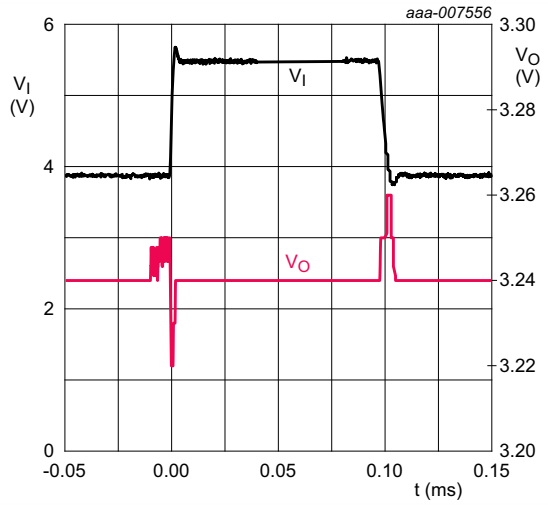
Line regulation response is the capability of the circuit to maintain the nominal output voltage while varying the input voltage.

$$Line\ regulation\ (\%/V) = \frac{\Delta V_O}{\Delta V_I} \times \frac{100}{V_O} \quad (1)$$



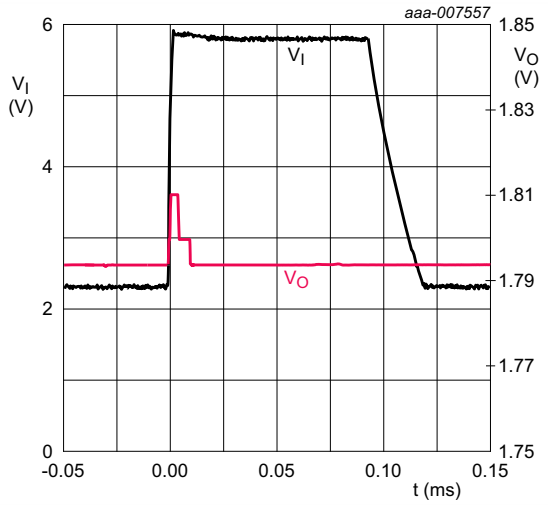
$V_{O(nom)}$ = 1.8 V; I_O = 300 mA; $t_r = t_f$ = 2 µs; $C_{L(ext)}$ = 1 µF; $C_{ext(IN)}$ = 1 µF

Fig 12. Line regulation for LD6935L/3318x



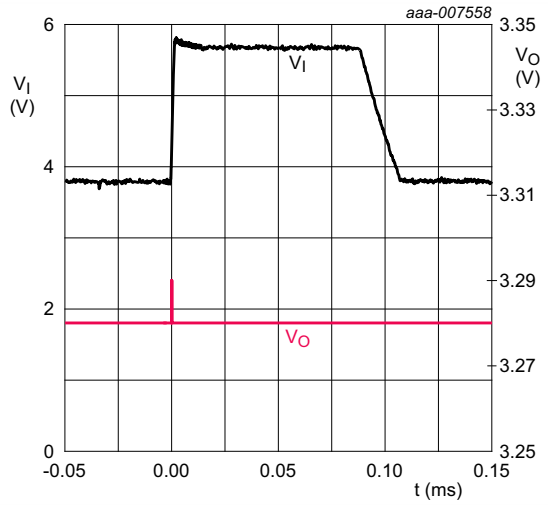
$V_{O(nom)}$ = 3.3 V; I_O = 300 mA; $t_r = t_f$ = 2 µs; $C_{L(ext)}$ = 1 µF; $C_{ext(IN)}$ = 1 µF

Fig 13. Line regulation for LD6935L/3318x



$V_{O(nom)}$ = 1.8 V; I_O = 1 mA; $t_r = t_f$ = 2 µs; $C_{L(ext)}$ = 1 µF; $C_{ext(IN)}$ = 1 µF

Fig 14. Line regulation for LD6935L/3318x



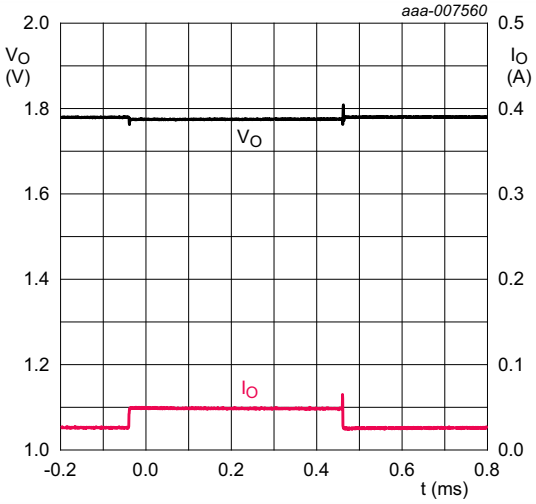
$V_{O(nom)}$ = 3.3 V; I_O = 1 mA; $t_r = t_f$ = 2 µs; $C_{L(ext)}$ = 1 µF; $C_{ext(IN)}$ = 1 µF

Fig 15. Line regulation for LD6935L/3318x

9.6 Load regulation

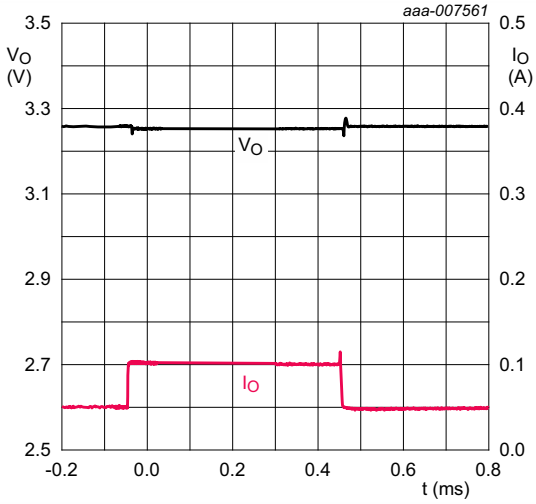
Load regulation is the capability of the circuit to maintain the nominal output voltage while varying the output load current.

$$Load\ regulation\ (\%/mA) = \frac{\frac{\Delta V_O}{V_{O(nom)}} \times 100}{\Delta I_O} \quad (2)$$



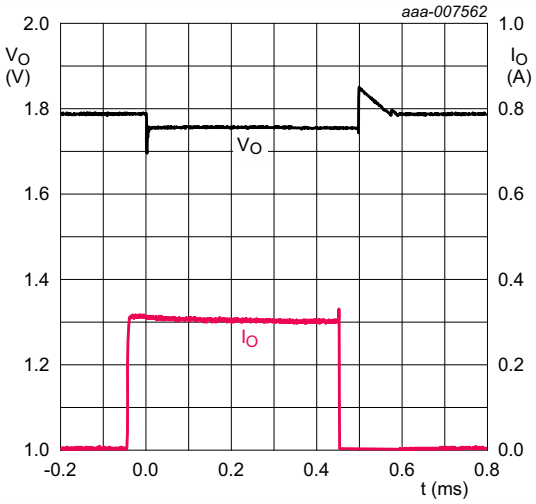
$V_{O(nom)}$ = 1.8 V; I_O = 50 mA to 100 mA; $t_r = t_f$ = 2 µs; $C_{L(ext)}$ = 1 µF; $C_{ext(IN)}$ = 1 µF

Fig 16. Load regulation for LD6935L/3318x



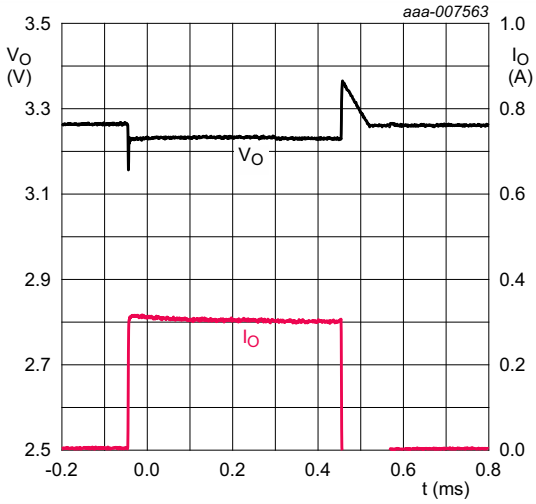
$V_{O(nom)}$ = 3.3 V; I_O = 50 mA to 100 mA; $t_r = t_f$ = 2 µs; $C_{L(ext)}$ = 1 µF; $C_{ext(IN)}$ = 1 µF

Fig 17. Load regulation for LD6935L/3318x



$V_{O(nom)}$ = 1.8 V; I_O = 0 mA to 300 mA; $t_r = t_f$ = 2 µs; $C_{L(ext)}$ = 1 µF; $C_{ext(IN)}$ = 1 µF

Fig 18. Load regulation for LD6935L/3318x

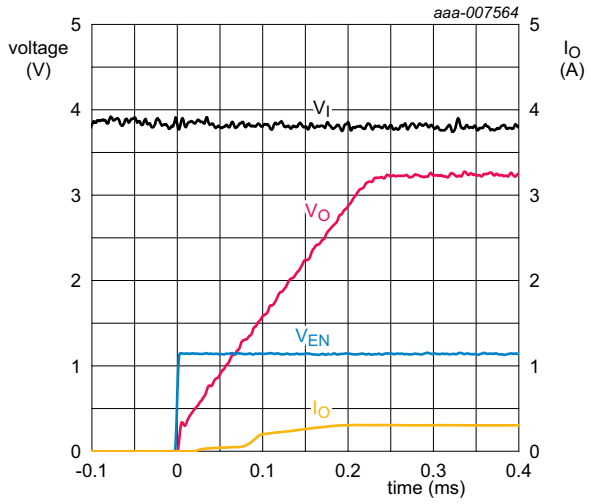


$V_{O(nom)}$ = 3.3 V; I_O = 50 mA to 300 mA; $t_r = t_f$ = 2 µs; $C_{L(ext)}$ = 1 µF; $C_{ext(IN)}$ = 1 µF

Fig 19. Load regulation for LD6935L/3318x

9.7 Start-up, inrush current

Start-up time defines the time needed for the LDO to achieve 95 % of its typical output voltage level after activation via the enable pin.



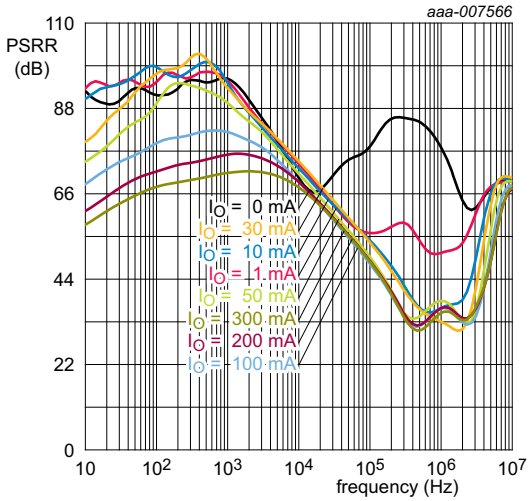
$V_{O(nom)}$ = 3.3 V; I_O = 300 mA; $C_{L(ext)}$ = 1 µF; $C_{ext(IN)}$ = 1 µF

Fig 20. Start-up and inrush current for LD6935L/3318x

9.8 Power Supply Rejection Ratio (PSRR)

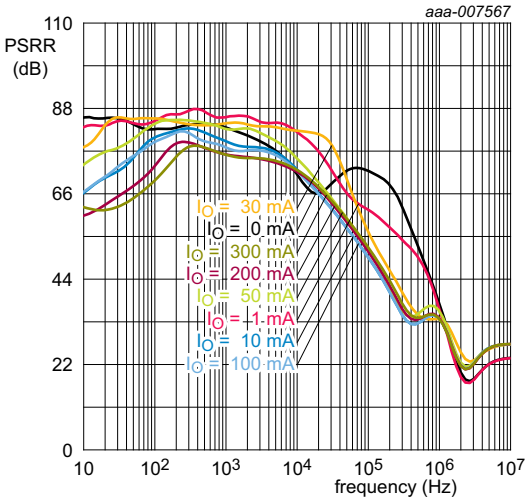
PSRR stands for the capability of the regulator to suppress unwanted signals on the input voltage like noise or ripples.

$$PSRR\ (dB) = (-20)log\frac{V_{O(ripple)}}{V_{I(ripple)}}$$ for all frequencies.



$V_{O(nom)}$ = 1.8 V; $C_{L(ext)}$ = 1 µF; $C_{ext(IN)}$ = 1 µF

Fig 21. PSRR for LD6935L/3318x



$V_{O(nom)}$ = 3.3 V; $C_{L(ext)}$ = 1 µF; $C_{ext(IN)}$ = 1 µF

Fig 22. PSRR for LD6935L/3318x

10. Application information

10.1 Input and output capacitor values

The devices require external capacitors at the output to guarantee a stable regulator behavior. Also an input capacitor is recommended to keep the input voltage stable. These capacitors should not under-run the specified minimum Equivalent Series Resistance (ESR).

The absolute value of the total capacitance attached to the output pins OUT1 and OUT2 influences the shutdown time ($t_{sd(reg)}$) of the devices.

Table 10. External load capacitor

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$C_{ext(IN)}$	external capacitance on pin IN	pin IN1 and IN2		0.7	1.0	-	µF
$C_{L(ext)}$	external load capacitance		[1]	0.7	1.0	-	µF
ESR	equivalent series resistance			5	-	500	mΩ

[1] The minimum value of capacitance for stability and correct operation is 0.7 µF. The capacitor tolerance should be ±30 % or better over the temperature range. The full range of operating conditions for the capacitor in the application should be considered during device selection to ensure that this minimum capacitance specification is met. The recommended capacitor type is X7R to meet the full device temperature specification of −40 °C to +125 °C.

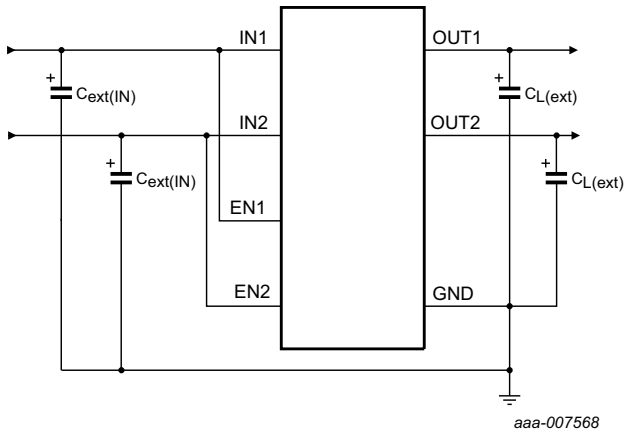


Fig 23. Application diagram

10.2 Optional delay circuit

The two enable input pins EN1 and EN2 allow a control of both LDOs. In case the availability of General-Purpose Input/Output (GPIO) pins is limited, the optional delay circuit of -D version can be used to control both LDOs at once without the drawback of doubled inrush current. When both enable signals EN1 and EN2 are activated simultaneously, the delay circuit delays the activation of LDO2 and postpones the associated inrush current. The LDO2 is only active when LDO1 is set to HIGH.

Table 11. Truth table output mode with delay circuit

EN1	EN2	LDO1 output	LDO2 output
LOW	LOW	OFF	OFF
HIGH	LOW	ON	OFF
LOW	HIGH	OFF	OFF
HIGH	HIGH	ON	ON

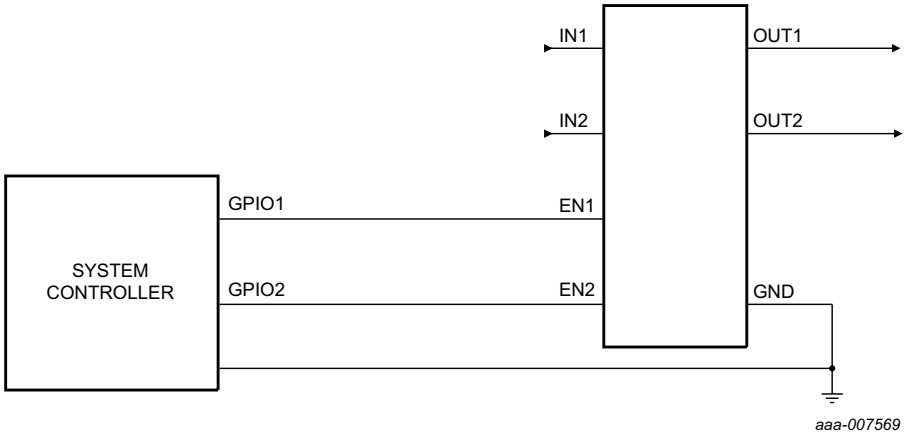


Fig 24. Flexible control with two separate GPIO signals

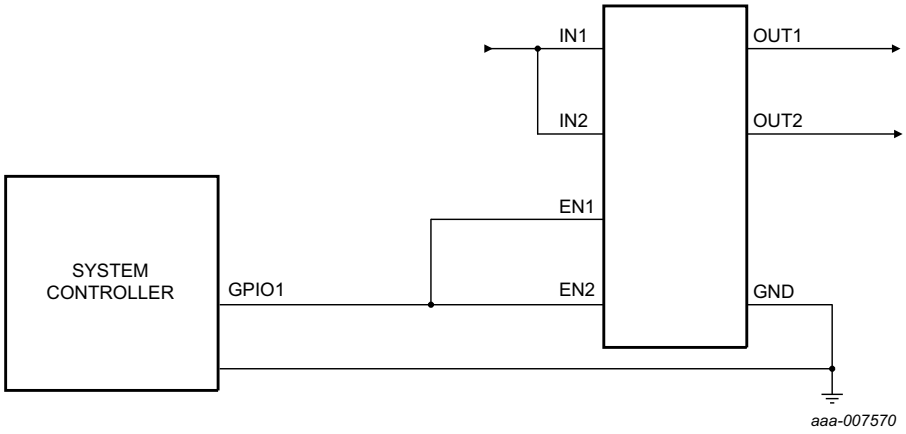


Fig 25. Control with one GPIO signal and delay circuit of -PD version

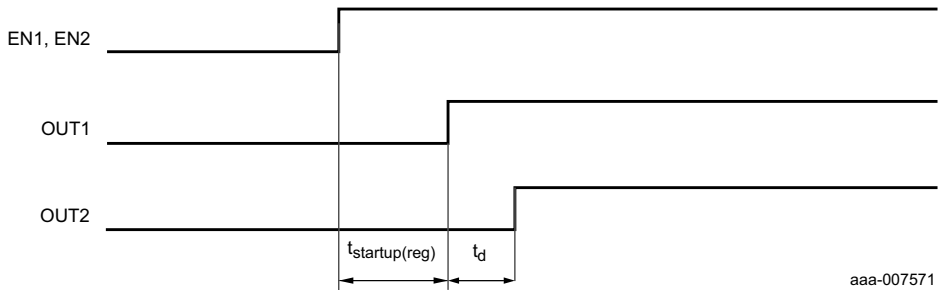


Fig 26. Timing diagram for delay circuit of -PD version

11. Test information

11.1 Quality information

This product has been qualified in accordance with *NX1-00023 NXP Semiconductors Quality and Reliability Specification* and is suitable for use in consumer applications.

12. Marking

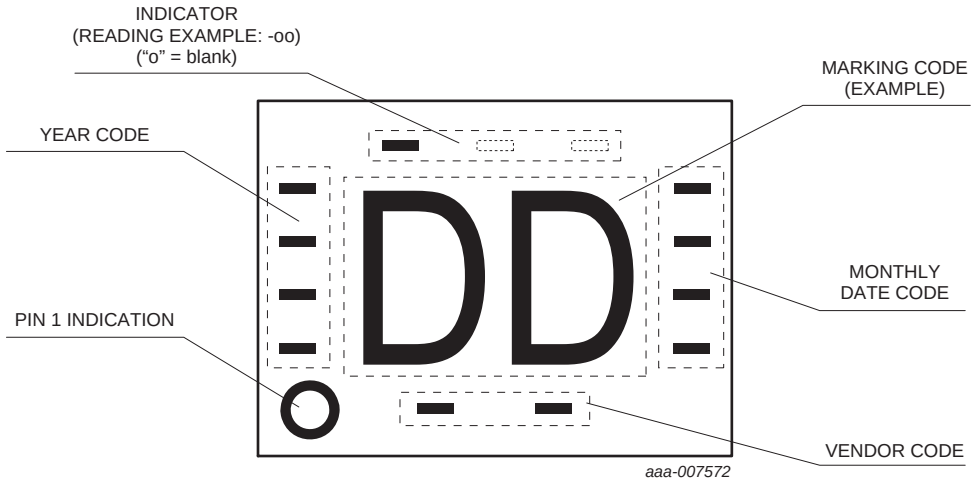


Fig 27. Marking DFN1612-8 (SOT1225)

Table 12. Marking code and indicator of high-ohmic output

Type number	$V_{O(nom)}$	Marking code	Indicator
LD6935L/2828H	2.8 V / 2.8 V	AK	oo-
LD6935L/3318H	3.3 V / 1.8 V	AE	oo-

Table 13. Marking code and indicator of pull-down output

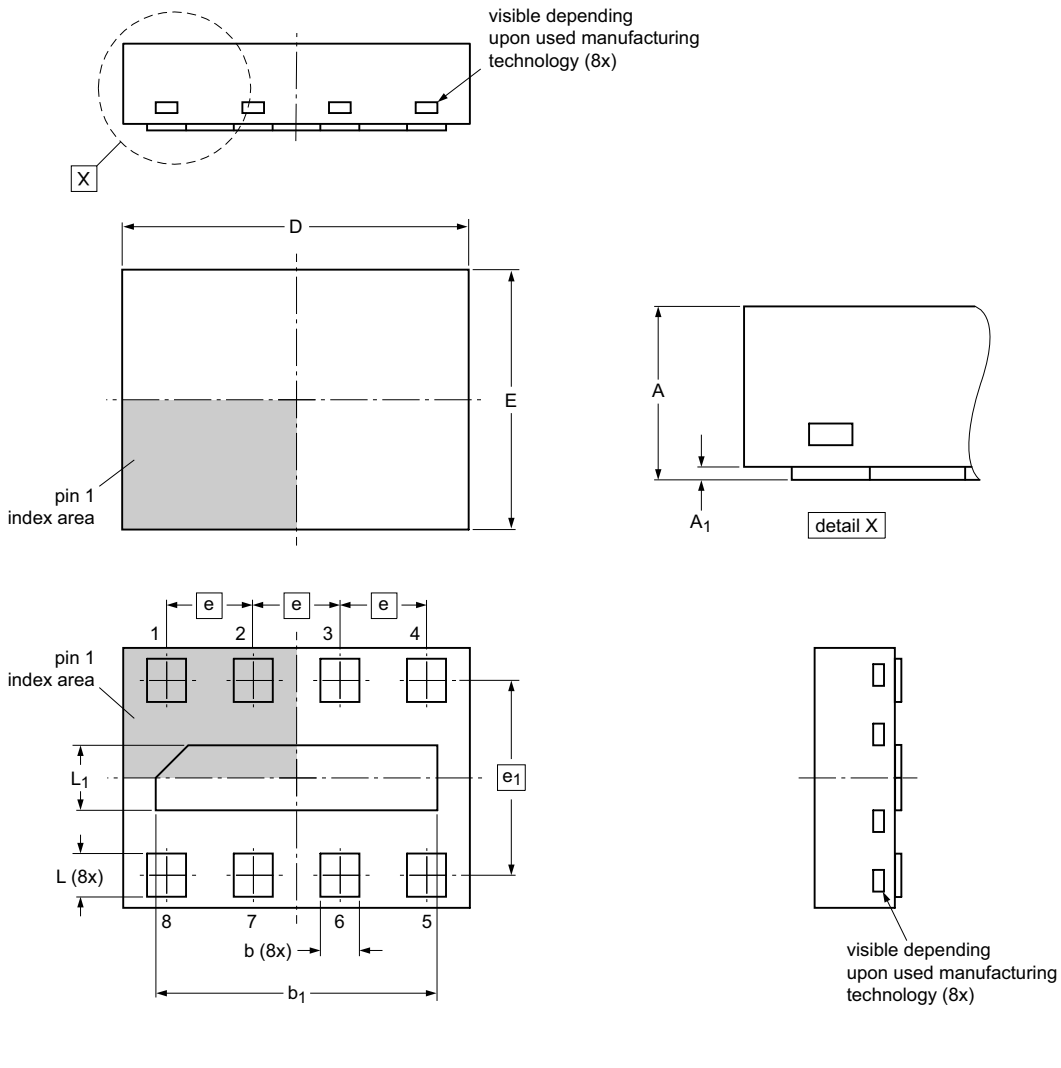
Type number	$V_{O(nom)}$	Marking code	Indicator
LD6935L/1818P	1.8 V / 1.8 V	AR	-oo
LD6935L/2828P	2.8 V / 2.8 V	AK	-oo
LD6935L/3318P	3.3 V / 1.8 V	AE	-oo
LD6935L/3328P	3.3 V / 2.8 V	AC	-oo
LD6935L/3333P	3.3 V / 3.3 V	AA	-oo

Table 14. Marking code and indicator of pull-down output with delay circuit

Type number	$V_{O(nom)}$	Marking code	Indicator
LD6935L/3118PD	3.1 V / 1.8 V	AU	o-o

13. Package outline

DFN1612-8: plastic extremely thin small outline package; no leads; 8 terminals; body 1.6 x 1.2 x 0.4 mm **SOT1225**



Dimensions (mm are the original dimensions)

Unit		A	A_1	D	E	e_1	e	b_1	b	L_1	L
	min	0.34		1.55	1.15			1.27	0.15	0.27	0.17
mm	nom	0.37		1.60	1.20	0.9	0.4	1.30	0.18	0.30	0.20
	max	0.40	0.04	1.65	1.25			1.35	0.23	0.35	0.25

Note
1. Dimension A is including plating thickness.

sot1225_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1225						~~11-11-09~~ 12-06-11

Fig 28. Package outline DFN1612-8 (SOT1225)

14. Packing information

14.1 Packing methods

Table 15. Packing methods

Type number	Package	Description	Orientation [1]	12NC ending	Packing quantity
LD6935L	SOT1225	4 mm pitch, 5.4 mm tape and reel	Q1	115	<tbd>

[1] For further information about orientation, see Section 14.2.

14.2 Carrier tape information

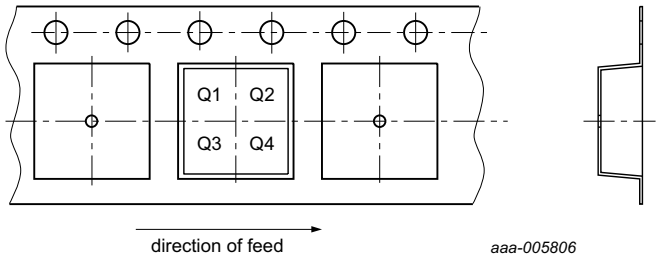


Fig 29. Carrier tape

Table 16. Orientations

Orientation	Meaning	Pin 1 location
Q1	quadrant 1	upper left
Q2	quadrant 2	upper right
Q3	quadrant 3	lower left
Q4	quadrant 4	lower right

15. Soldering

Footprint information for reflow soldering of DFN1612-8 package **SOT1225**

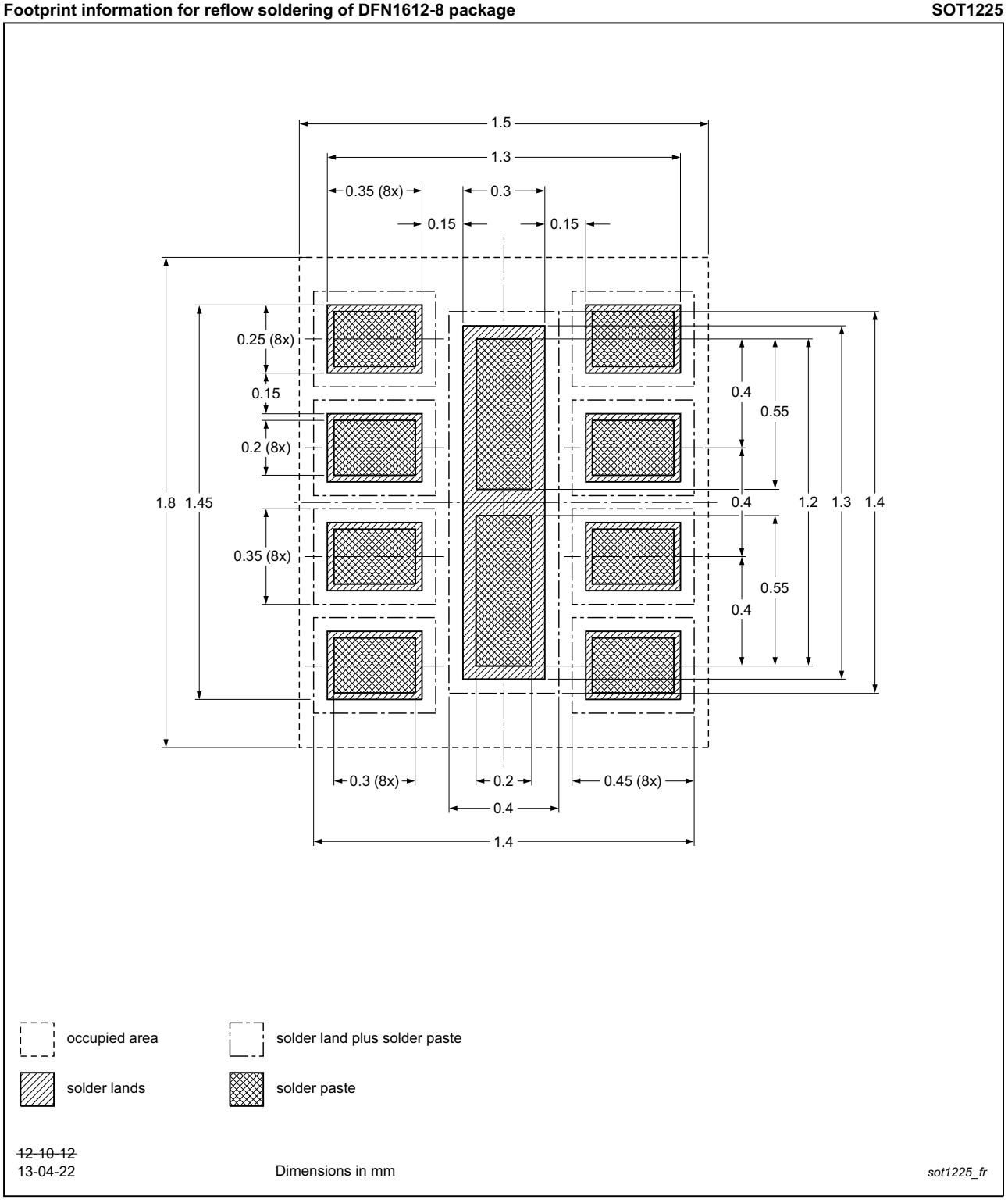
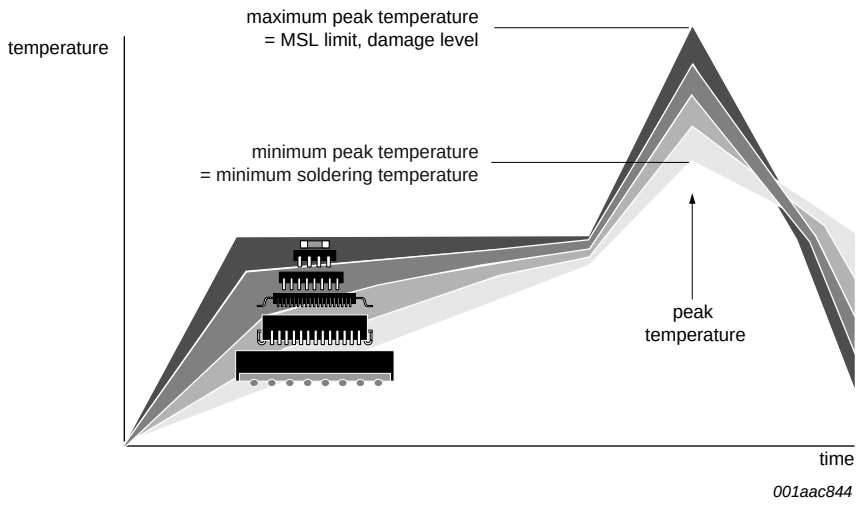


Fig 30. Soldering footprint DFN1612-8 (SOT1225)

16. PCB assembly guidelines for Pb-free soldering

Table 17. Assembly recommendations

Parameter	Value or specification
Solder screen thickness	100 μm (0.004 inch)
Solder paste: Pb-free	SnAg (3 % to 4 %); Cu (0.5 % to 0.9 %)
Solder to flux ratio	50 : 50
Solder reflow profile	see Figure 31



The device can withstand at least three reflows at this profile.

Fig 31. Pb-free solder reflow profile

Table 18. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{reflow(peak)}$	peak reflow temperature		230	-	260	°C
t_1	time 1	soak time	60	-	180	s
t_2	time 2	time during T ≥ 250 °C	-	-	30	s
t_3	time 3	time during T ≥ 230 °C	10	-	50	s
t_4	time 4	time during T > 217 °C	30	-	150	s
t_5	time 5		-	-	540	s
dT/dt	rate of change of temperature	cooling rate	-	-	–6	°C/s
		preheat	2.5	-	4.0	°C/s

17. Revision history

Table 19. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LD6935_SER v.1	20130529	Preliminary data sheet	-	-

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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20. Contents

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