STEP-UP, FOR LCD BIAS SUPPLY, 3-CHANNEL SWITCHING REGULATOR

S-8335 Series

The S-8335 Series is a bias supply IC for a Multi Line Addressing (MLA) driven LCD using a dual-line simultaneous selection mode. This IC supports medium-sized LCD panels. Two step-up type and one inverter type PFM control CMOS switching regulators supply the required positive or negative power to the two MLA-driven LCD common drivers and segment drivers. Because of its CMOS structure, the current consumption of the S-8335 Series is extremely low, which makes it ideal for the LCD power supply of portable equipment that requires low power consumption. Also, an extremely low power consumption LCD module can be created by using the S-8335 Series with the LCD common driver (HD66523R*1: Manufactured by Hitachi, Ltd.) and segment driver (HD66522*1: Manufactured by Hitachi, Ltd.).

*1:These drivers are able to support 1/240duty and 1/200duty.

■ Features

- Supports four types of LCD panels (1/240 duty, 1/200 duty, 1/160 duty, and 1/120 duty).
- Input voltage range: 2.4 to 5.0 V (The S-8335 can be driven by a single direct-coupled lithium battery.)
- Output voltage range
  Common driver positive power supply (VRH) output voltage range(typ.value)
  8.91 to 16.59 V (S-8335A240FT)
  8.22 to 15.30 V (S-8335A200FT)
  7.48 to 13.93 V (S-8335A160FT)
  6.66 to 12.41 V (S-8335A120FT)
  (This supply can be varied by on-chip 6-bit electric volume. Power MOSFET is built in.)
  Common driver negative power supply (VRL) output voltage range(typ.value)
  -6.87 to -12.80 V (S-8335A240FT)
  -6.18 to -11.49 V (S-8335A200FT)
  -5.44 to -10.13 V (S-8335A160FT)
  -4.61 to -8.59 V (S-8335A120FT)
  Segment driver positive power supply (VCH) output voltage range 2.0 to 3.8 V
  Segment driver intermediate potential (VM) output voltage range 1.0 to 1.9 V
  Icon positive power supply (VICON) output voltage range 1.0 to 2.2 V (This supply can be set arbitrarily by external resistors.)
- Low current consumption
  100 μA typ. (mode 1, V_{BAT} = 3 V)
  10 μA typ. (mode 2, V_{BAT} = 3 V)
  1 μA max. (mode 3, V_{BAT} = 3 V)
- Triple operation mode function: Triple mode switching according to 2-bit input
  Mode 1: Normal operation
  Mode 2: Icon mode (reference voltage circuit- and regulator S-only operation)
  Mode 3: Standby mode (power off)
- Power-off function
  Stops step-up or step-down operation and short circuits VRH and VRL to VSS by on-chip and external Nch transistors.
- Soft-start function: This function can be set according to an external capacitor (CSS).
- Oscillation frequency: 100 kHz ± 20 kHz, Duty = 50%
- Lead-free products

■ Applications

- Power supply for medium-sized LCD panel

■ Package Name

- 24-pin TSSOP package (PKG diagram code: FT024-A)

■ Block Diagram

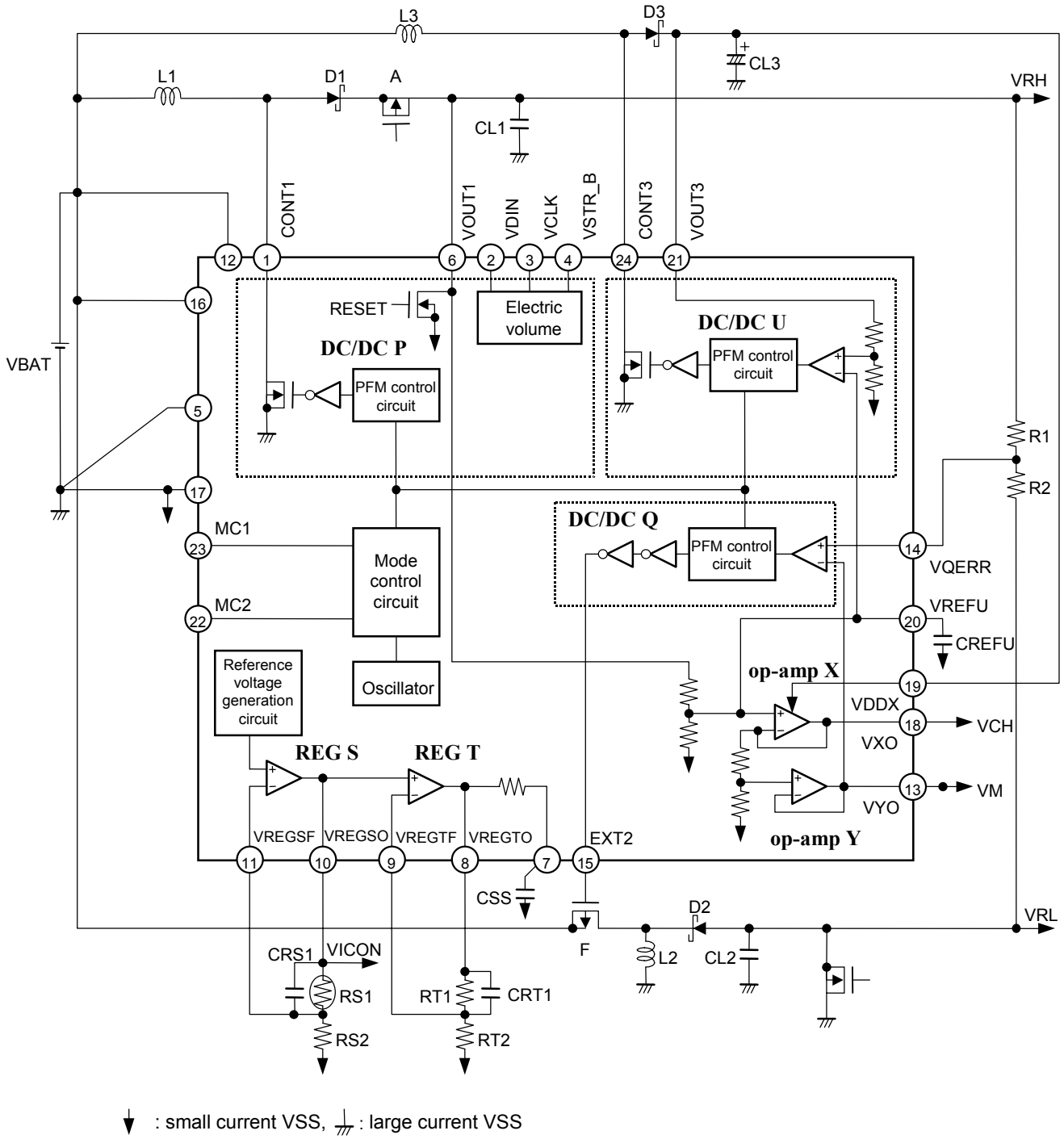


Figure 1 Block Diagram

Note:

Except for op-amp X, all of the power for the internal circuits of the S-8335 Series is supplied by the VBAT pins. The power supply for op-amp X uses V_{OUT3}, which is generated by stepping up V_{BAT} using DC/DC U. Short-circuit the VOUT3 and VDDX pins as shown in the figure above.

■ Selection Guide

1. Product name

S – 8 3 3 5 A XXX FT – T B – G

- FT: Package name (abbreviation)
- XXX: Product type
  - 240: 1/240 duty support
  - 200: 1/200 duty support
  - 160: 1/160 duty support
  - 120: 1/120 duty support

2. Product list

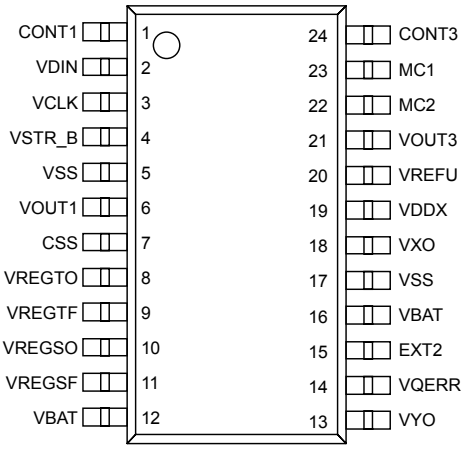
S-8335AXXXFT Series	Bias Ratio	Common Driver Positive Power Supply VRH Output Voltage Range [V]		Common Driver Negative Power Supply VRL Output Voltage Range [V]	
		V_{RH_min}	V_{RH_max}	V_{RL_min}	V_{RL_max}
S-8335A240FT-TB-G	8.75	8.91	16.59	−6.87	−12.80
S-8335A200FT-TB-G	8.04	8.22	15.30	−6.18	−11.49
S-8335A160FT-TB-G	7.33	7.48	13.93	−5.44	−10.13
S-8335A120FT-TB-G	6.50	6.66	12.41	−4.61	−8.59

Note: V_{RH_min} and V_{RL_min} indicate the typical value of the VRH and VRL output voltage, respectively, when the electric volume is set to the minimum, and V_{RH_max} and V_{RL_max} indicate the typical value of the VRH and VRL output voltage, respectively, when the electric volume is set to the maximum. Also, V_{RH_max} is obtained from $V_{RETGO} \times 7.136$ and V_{RH_min} is obtained from $V_{RETGO} \times 3.832$, where V_{RETGO} is the regulator T output voltage.

■ Pin Assignment

24-pin TSSOP Package

Top view



Pin No.	Pin Name	Function
1	CONT1	External inductor 1 connection pin
2	VDIN	Electric volume data input pin
3	VCLK	Electric volume clock input pin
4	VSTR_B	Electric volume strobe signal input pin
5	VSS	GND pin
6	VOUT1	Switching regulator P output voltage pin
7	CSS	Soft start capacitor connection pin
8	VREGTO	Regulator T output pin
9	VREGTF	Regulator T feedback input pin
10	VREGSO	Regulator S output pin
11	VREGSF	Regulator S feedback input pin
12	VBAT	Power supply pin
13	VYO	OP amplifier Y output pin
14	VQERR	Switching regulator Q output voltage monitoring pin
15	EXT2	Switching regulator Q external transistor connection pin
16	VBAT	Power supply pin
17	VSS	GND pin
18	VXO	OP amplifier X output pin
19	VDDX	OP amplifier X power supply pin
20	VREFU	Switching regulator U internal reference voltage pin
21	VOUT3	Switching regulator U output voltage pin
22	MC2	Operating mode control pin 2
23	MC1	Operating mode control pin 1
24	CONT3	External inductor 3 connection pin

■ Absolute Maximum Ratings

(Unless otherwise specified: T_{OPR}=25°C)

Parameter	Symbol	Ratings	Unit
VBAT pin voltage	V_{BAT}	8	V
CONT1 pin voltage	V_{CONT1}	−0.3 to +20	V
CONT1 pin current	I_{CONT1}	300	mA
VOUT1 pin voltage	V_{OUT1}	−0.3 to +20	V
EXT2 pin voltage	V_{EXT2}	−0.3 to V_{BAT}+20	V
EXT2 pin current	I_{EXT2}	±50	mA
CONT3 pin voltage	V_{CONT3}	−0.3 to +8	V
CONT3 pin current	I_{CONT3}	200	mA
VOUT3 pin voltage	V_{OUT3}	−0.3 to +8	V
VQERR pin voltage	V_{QERR}	−0.3 to +8	V
VDDX pin voltage	V_{DDX}	8	V
VXO pin voltage	V_{XO}	−0.3 to V_{DDX}+0.3	V
Other pin voltage		−0.3 to V_{BAT}+0.3	V
Power dissipation	P_D	650	mW
Operating temperature range	T_{OPR}	−20 to +70	°C
Storage temperature range	T_{STG}	−40 to +125	°C

Note: Although this IC incorporates an electrostatic protection circuit, the user is urged to avoid subjecting the circuit to an extremely high static electricity or voltage in excess of its performance.

■ Electrical Characteristics

Note:

The data specifications are based on measured results using recommended peripheral parts (see ■ **Recommended Peripheral Parts**).

Common

(Unless otherwise specified: V_{BAT} = 3.0 V, T_{OPR} = 25°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Measure-ment Circuit
Input voltage	V_{BAT}		2.4	3.0	5.0	V	–
Mode 1 current consumption for full oscillation	I_{MC11}	Current flowing from power supply pin V_{BAT}. Only regulator S and T resistance externally. Maximum setting for electric volume. Output voltage of DC/DC P, U, and Q are each setting value × 0.9. CONT1 and CONT3 are pulled up to 3 V via a 300 Ω resistor.	–	100	200	μA	1
Mode 1 current consumption for stopped oscillation	I_{MC12}	Current flowing from power supply pin V_{BAT}. Only regulator S and T resistance externally. Maximum setting for electric volume. Output voltage of DC/DC P, U, and Q are each setting value × 1.2. CONT1 and CONT3 are pulled up to 3 V via a 300 Ω resistor.	–	40	90	μA	1
Mode 2 current consumption	I_{MC2}	Current flowing from power supply pin V_{BAT}. Only regulator S and T resistance externally. Output voltage of DC/DC P, U, and Q are 0 V. CONT1 and CONT3 are pulled up to 3 V via a 300 Ω resistor.	–	10	20	μA	1
Mode 3 current consumption	I_{MC3}	Current flowing from power supply pin V_{BAT}. Only regulator S and T resistance externally. Output voltage of DC/DC P, U, and Q are 0 V. CONT1 and CONT3 are pulled up to 3 V via a 300 Ω resistor.	–	–	1.0	μA	1
MC1, MC2, VDIN, VCLK, VSTR_B pin input voltage	V_{CH}		1.6	–	–	V	1
	V_{CL}		–	–	0.4	V	1

Oscillator Part

(Unless otherwise specified: V_{BAT} = 3.0 V, T_{OPR} = 25°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Measure-ment Circuit
Oscillation frequency	f_{OSC}		80	100	120	kHz	1
Duty ratio	Duty		40	50	60	%	1

VRH Generation Step-Up Type DC/DC P Part

(Unless otherwise specified: V_{BAT}=3.0 V, T_{OPR} = 25°C)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit	Measure-ment Circuit
Output voltage 1	V_{OUT11}	Electric volume at maximum, I_{OUT1} = 100 μA	For S-8335A240FT, V_{REGTO} = 2.325 V	16.180	16.590	17.009	V	2
			For S-8335A200FT, V_{REGTO} = 2.144 V	14.918	15.300	15.683	V	
			For S-8335A160FT, V_{REGTO} = 1.952 V	13.582	13.930	14.278	V	
			For S-8335A120FT, V_{REGTO} = 1.739 V	12.098	12.410	12.718	V	
Output voltage 2	V_{OUT12}	Electric volume at minimum, I_{OUT1} = 100 μA	For S-8335A240FT, V_{REGTO} = 2.325 V	8.688	8.910	9.134	V	2
			For S-8335A200FT, V_{REGTO} = 2.144 V	8.011	8.220	8.422	V	
			For S-8335A160FT, V_{REGTO} = 1.952 V	7.293	7.480	7.667	V	
			For S-8335A120FT, V_{REGTO} = 1.739 V	6.496	6.660	6.829	V	
Switching current	I_{SWP}	V_{CONT1} = 0.4 V		60	85	–	mA	1
Switching transistor leakage current	I_{SWQP}	For mode 3 (25°C)		–	–	1	μA	1
		For mode 3 (70°C)		–	–	10	μA	–
VOUT1 pin input current	I_{VOUT1}	For electric volume set to minimum		2	4	8	μA	1
VOUT1 pin sink current	I_{VOUT1L}	Mode 3, V_{OUT1} = 0.4 V		0.9	1.3	–	mA	1
Soft start time	T_{ss}	Time until the error amplifier reference voltage reaches 90% of the final value of the regulator T output voltage. C_{RT1}= 0.1 μF, C_{SS}= 0.01 μF		10	15	35	ms	1
Efficiency	EFFIP	Electric volume set to middle, I_{OUT1} = 1 mA		–	82	–	%	–

DC/DC P Electric Volume Part

(Unless otherwise specified: V_{BAT} = 3.0 V, T_{OPR} = 25°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Measure-ment Circuit
Electric volume adjustment range	V_{OUT}	For S-8335A240FT, V_{REGTO} = 2.325 V	8.91±2.5%	–	16.59±2.5%	V	2
		For S-8335A200FT, V_{REGTO} = 2.144 V	8.22±2.5%	–	15.30±2.5%	V	
		For S-8335A160FT, V_{REGTO} = 1.952 V	7.48±2.5%	–	13.93±2.5%	V	
		For S-8335A120FT, V_{REGTO} = 1.739 V	6.66±2.5%	–	12.41±2.5%	V	
Potential division precision			–	–	2.5	%	2
Electric volume resolution			–	1/63	–		2
Linearity error			–	–	1/2	LSB	2
Data setup time	t_{sc}		5.0	–	–	µs	–
Data hold time	t_{hc}		5.0	–	–	µs	–
VCLK pulse width	t_{dc}		0.5	4.17	–	µs	–
VCLK period	t_{tc}		5.0	8.33	–	µs	–
VCLK↓ to VSTR_B ↓	t_{ss}		5.0	–	–	µs	–
VSTR_B pulse width	t_{da}		5.0	–	–	µs	–
VSTR_B↑ to VCLK↑	t_{hs}		5.0	–	–	µs	–

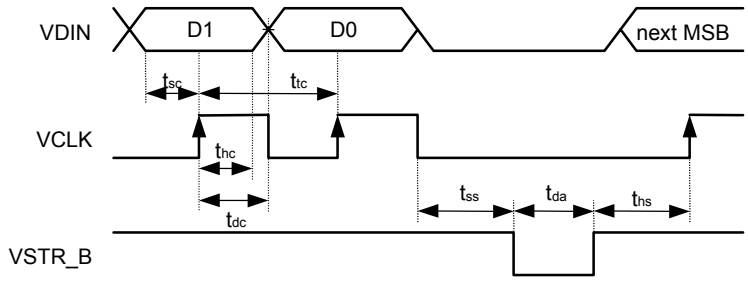


Figure 2 Clock Timing

VDIN	VCLK	VSTR_B	State
H	–	–	Data 1
L	–	–	Data 0
–	L to H	–	Load data in shift register
–	–	L	Load shift register contents in latch
–	–	H	Hold latch data

VRL Generation Inverter Type DC/DC Q Part

(Unless otherwise specified: V_{BAT} = 3.0 V, T_{OPR} = 25°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Measure-ment Circuit
Comparator offset	V_{QEROF}	V_{YO} = 1.45 V	−20	0	+20	mV	1
EXT2 pin output current	I_{EXT2H}	For $V_{EXT2} = V_{BAT}$ - 0.4 V	−5.3	−7.6	−	mA	1
	I_{EXT2L}	For V_{EXT2} = 0.4 V	7.4	10.5	−	mA	1
Efficiency	EFFIQ	Electric volume set to middle, I_{OUT2} = 1 mA	−	60	−	%	−

Step-up Type DC/DC U Part

(Unless otherwise specified: V_{BAT} = 3.0 V, T_{OPR} = 25°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Measure-ment Circuit
Output voltage	V_{OUT3}	For fixed V_{REFU} = 2.90 V, I_{OUT3} = 100 µA	2.97	3.05	3.12	V	2
Switching current	I_{SWU}	V_{CONT3} = 0.4 V	73	104	−	mA	1
Switching transistor leak current	I_{SWQU}	Mode 3	−	−	1.0	µA	1
VOUT3 pin off current	I_{VOUT3L}	Mode 3, V_{OUT3} = 0.4 V	−	−	0.5	µA	1
Efficiency	EFFIU	Electric volume set to middle, I_{OUT3} = 1 mA	−	95	−	%	−

OP Amplifier X Part

(Unless otherwise specified: V_{BAT} = 3.0 V, T_{OPR} = 25°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Measure-ment Circuit
Output voltage	V_{XO}	I_{OUTX} = 50 µA, V_{REFU} = 2.90 V	2.828	2.90	2.973	V	1
Output voltage 2	V_{XO2}	For 1mA output	V_{XO} - 0.08	−	V_{XO}	V	1
Current consumption	I_{SSX}		−	10	20	µA	1
VXO pin sink current	I_{VXOL}	Mode 3, V_{XO} = 0.4 V	0.46	0.66	−	mA	1

OP Amplifier Y Part

(Unless otherwise specified: V_{BAT} = 3.0 V, T_{OPR} = 25°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Measure-ment Circuit
Output voltage precision	V_{YOD}	= (V_{XO}-V_{YO})/V_{YO}, no load at Y, I_{OUTX} = 50 µA	0.98	−	1.02		1
VYO pin sink current	I_{VYOL}	Mode 3, V_{YO} = 0.4 V	0.46	0.66	−	mA	1

Regulator S Part

(Unless otherwise specified: V_{BAT} = 3.0 V, T_{OPR} = 25°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Measure-ment Circuit
Output voltage	V_{REGSO}	I_{OUTS} = 50 μA, RS1 = 210 kΩ, RS2 = 270 kΩ	1.576	1.6	1.624	V	1
Output voltage temperature coefficient	ΔV_{REGSO} /(V_{REGSO} • ΔT_{OPR})	T_{OPR} = -20°C to +70°C (when no RS1, RS2 temperature characteristics are taken into account)	–	±50	–	ppm/°C	–
VREGSO pin sink current	$I_{VREGSOL}$	Mode 3, V_{REGSO} = 0.4 V	0.40	0.57	–	mA	1

Regulator T Part

(Unless otherwise specified: V_{BAT} = 3.0 V, T_{OPR} = 25°C)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit	Measure-ment Circuit
Output voltage	V_{REGTO}	For fixed V_{REGSO} = 1.6 V, I_{OUTT}=50 μA. For RT1, RT2 values, see Recom-mended Peripheral Parts.	S-8335A240FT	2.290	2.325	2.360	V	1
			S-8335A200FT	2.112	2.14	2.176	V	
			S-8335A160FT	1.923	1.95	1.981	V	
			S-8335A120FT	1.713	1.74	1.765	V	
VREGTO pin sink current	$I_{VREGTOL}$	Mode 3, V_{REGSO} = 0.4 V		0.46	0.65	–	mA	1

■ Recommended Peripheral Parts (When V_{ICON}=1.6 V)

Part	Value	Unit	Model No.	Remark
L1, L2, L3	150	μH	CDRH5D18-151	Manufactured by Sumida Electric Co., Ltd.
D1, D2, D3			MA720	Manufactured by Matsushita Electric Components Co., Ltd. (Schottky type)
CL1	2.2	μF	CM316W5R225K25A	Ceramic type
CL2	2.2	μF	CM316W5R225K25A	Ceramic type
CL3	10	μF	F930J106MA	Tantalum type
MOSFET A			2SJ356	Pch MOSFET manufactured by NEC
MOSFET F			TM5211	Pch MOSFET manufactured by Toyoda Automatic Loom Works, Ltd.
MOSFET C			2SJ463A	Pch MOSFET manufactured by NEC
MOSFET D, E, G			2SK3019	Nch MOSFET manufactured by ROHM
CL4	1	μF	CM21B105K10A	Ceramic type
CL5	1	μF	CM21B105K10A	Ceramic type
CL6	1	μF	CM21B105K10A	Ceramic type
CL7	1	μF	CM21B105K10A	Ceramic type
CREFU	2200	pF	CM105W5R222M10A	Ceramic type
CSS	0.01	μF	CM105W5R103M10A	Ceramic type
CR1, CR2	0.01	μF	CM105W5R103K25A	Ceramic type
CRS1	–	μF		Ceramic type (capacitance added only when regulator S oscillates)
CRT1	0.1	μF	CM105W5R104M10A	Ceramic type
CVBAT1	1	μF	CM105Y5V105Z10A	Ceramic type
CVBAT2	1	μF	CM105Y5V105Z10A	Ceramic type
CMC1, CMC2, CMC3	0.1	μF	CM105Y5V104Z10A	Ceramic type
CDIN, CCLK, CSTR_B	1	μF	CM105Y5V105Z10A	Ceramic type
R1, R2	1	MΩ		±0.5% precision
RS1	210	kΩ		(100 + 110) kΩ, 100 kΩ replaced by thermistor. Ishizuka Electronics Corporation thermistor 104HT (100 kΩ).
RS2	270	kΩ		Use when RS1 + RS2 > 100 kΩ
RT1	68	kΩ		S-8335A240FT (Use when RT1 + RT2 > 185 kΩ)
	51	kΩ		S-8335A200FT (Use when RT1 + RT2 > 110 kΩ)
	33	kΩ		S-8335A160FT (Use when RT1 + RT2 > 80 kΩ)
	13	kΩ		S-8335A120FT (Use when RT1 + RT2 > 65 kΩ)
RT2	150	kΩ		
RA1	470	kΩ		
RA2	150	kΩ		
RA3	150	kΩ		

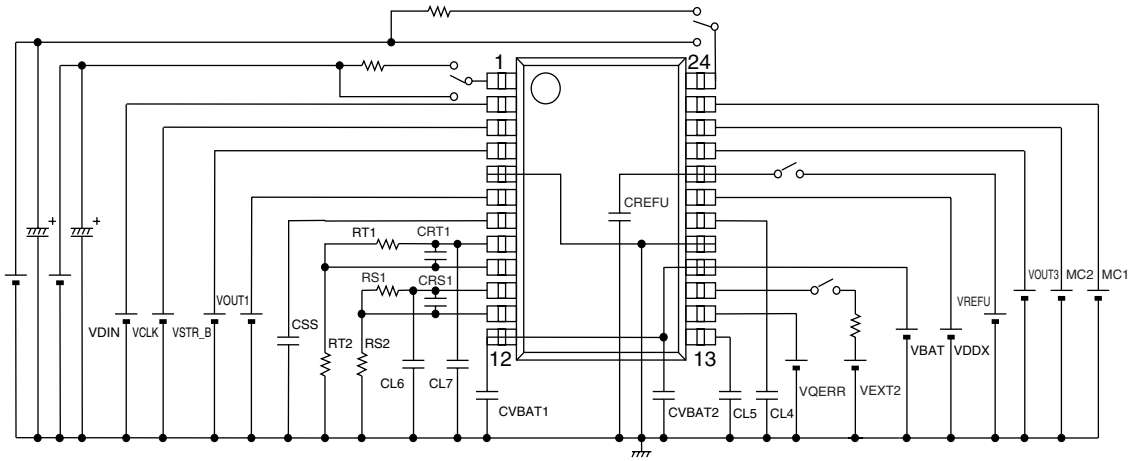
Note 1: The regulator S input (reference voltage generation circuit output) voltage has been trimmed to 0.9 V when shipped. Also, the external resistance RS1 and RS2 of the recommended peripheral parts have been set so that V_{ICON}=1.6 V. When a V_{ICON} value other than 1.6 V is used, select the resistance RS1 and RS2 values to match the V_{ICON} voltage used. Also change the RT1 and RT2 values at the same time, because the RT1 and RT2 values are selected based on V_{ICON}=1.6 V.

Note 2: CRS1 is not usually necessary. Add the capacitance only when regulator S is oscillating. Evaluate the actual device using capacitance value on the order of 0.1 μF.

Note 3: The output voltage precision does not include external resistance dispersion.

■ Measurement Circuits

1:



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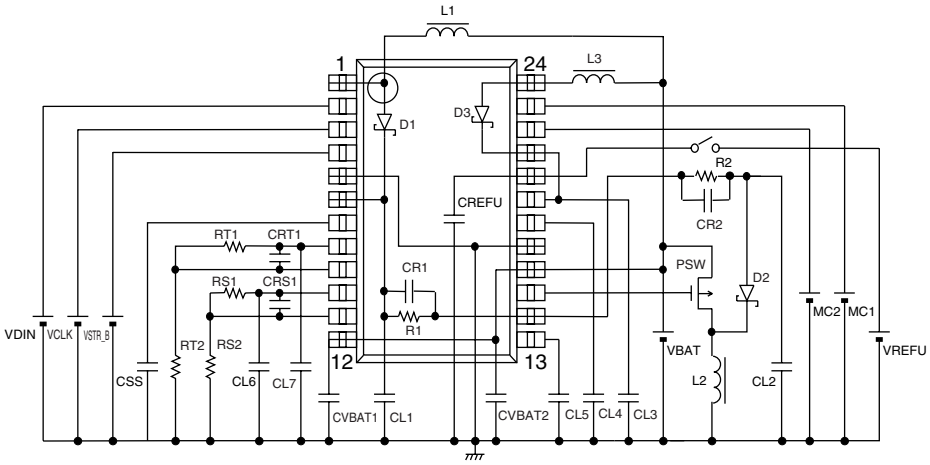


Figure 3 Measurement Circuits

■ Operation

The S-8335 Series has two step-up type and one inverter type CMOS on-chip switching regulators. These switching regulators employ the pulse frequency modulation (PFM) method to provide low current consumption features.

1. Operation Overview

The output of the reference voltage generation circuit is the input to regulator S. The output of regulator S is the input to regulator T. After the extremely steep rise has been blunted by an RC low-pass filter, the output of regulator T becomes the DC/DC P reference voltage. The DC/DC P output (pin name: VOUT1) that is controlled by the electric volume is obtained based on this reference voltage. The DC/DC P output becomes the common driver positive power supply (VRH).

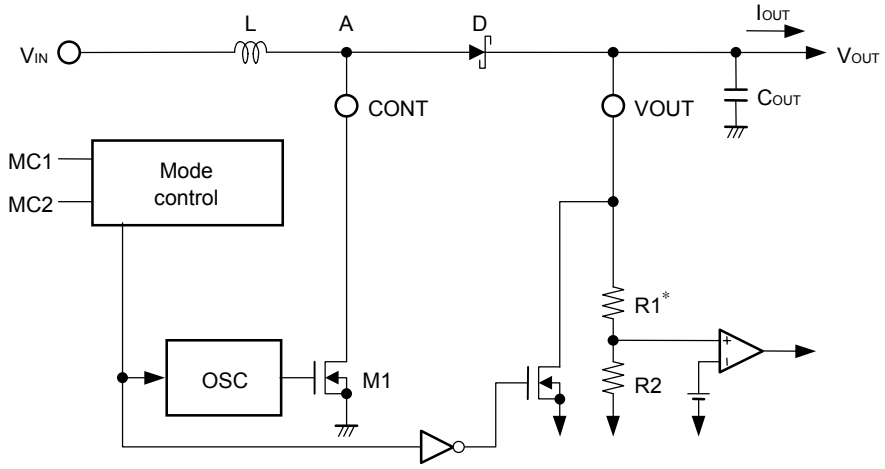
VRH is divided by internal resistors and becomes the input of OP amplifier X. The output (pin name: VXO) of OP amplifier X becomes the segment driver positive power supply (VCH).

Also, the input voltage of OP amplifier X becomes the reference voltage of the DC/DC U error amplifier. The DC/DC U output (pin name: VOUT3) is obtained so that it becomes 1.05 times larger than this reference voltage. The DC/DC U output voltage can be used for the OP amplifier X power supply voltage.

VCH is divided by internal resistors and becomes the input of OP amplifier Y. The output (pin name: VYO) of OP amplifier Y becomes the segment driver intermediate potential (VM).

VM becomes the reference voltage of the DC/DC Q error amplifier. DC/DC Q oscillates and VRL is obtained so that the common driver negative power supply (VRL) and VRH are symmetric around VM.

2. Step-up type switching regulators (DC/DC P and DC/DC U)



*: In DC/DC P, R1 is a variable resistance controlled by the electric volume.

Figure 4 DC/DC P and DC/DC U

The fundamental equations {(1) to (7)} of the step-up type regulators are shown below (see Figure 4).

CONT pin voltage (V_A) immediately after M1 is turned on (I_L, which is the current that flows to L, is zero):

$$V_A = V_S \quad \text{.....} \quad (1)$$

(V_S: Unsaturated voltage of M1)

Change in I_L with time:

$$\frac{dI_L}{dt} = \frac{V_L}{L} = \frac{V_{IN} - V_S}{L} \quad \text{.....} \quad (2)$$

Result of integrating the above equation (I_L):

$$I_L = \left(\frac{V_{IN} - V_S}{L} \right) \cdot t \quad \text{.....} \quad (3)$$

The current I_L flows during time t_{ON}. This time (t_{ON}) is determined according to the oscillation frequency of OSC.

Peak current (I_{PK}) after t_{ON}:

$$I_{PK} = \left(\frac{V_{IN} - V_S}{L} \right) \cdot t_{ON} \quad \text{.....} \quad (4)$$

The energy stored in L at this time is represented by $1/2 \cdot L(I_{PK})^2$.

Next, when M1 is turned off (t_{OFF}), the energy stored in L is emitted through a diode, and a counter voltage (V_L) is generated.

V_L:

$$V_L = (V_{OUT} + V_D) - V_{IN} \quad \text{.....} \quad (5)$$

(V_D: Diode forward voltage)

The CONT pin voltage rises by the voltage corresponding to $V_{OUT} + V_D$.

Change with time of current (I_L) that flows to V_{OUT} through a diode during time t_{OFF}:

$$\frac{dI_L}{dt} = \frac{V_L}{L} = \frac{V_{OUT} + V_D - V_{IN}}{L} \quad \text{.....} \quad (6)$$

Result of integrating the above equation:

$$I_L = I_{PK} - \left(\frac{V_{OUT} + V_D - V_{IN}}{L} \right) \bullet t \quad \text{.....} \quad (7)$$

During t_{ON}, the energy is stored in L and not transmitted to V_{OUT}. When output current (I_{OUT}) flows from V_{OUT}, the capacitor (C_{OUT}) energy is used. As a result, the C_{OUT} pin voltage decreases and reaches its lowest value after time t_{ON}. When M1 is turned off, the energy stored in L is transmitted through the diode to C_{OUT}, and the C_{OUT} pin voltage rises dramatically. V_{OUT} is a time function that indicates the maximum value (ripple voltage: V_{P-P}) when the current flowing through the diode to V_{OUT} matches the load current I_{OUT}.

This ripple voltage value is calculated below.

I_{OUT} when the time from immediately after t_{ON} until V_{OUT} reaches its highest level is set to t_1:

$$I_{OUT} = I_{PK} - \left(\frac{V_{OUT} + V_D - V_{IN}}{L} \right) \bullet t_1 \quad \text{.....} \quad (8)$$

$$\therefore t_1 = (I_{PK} - I_{OUT}) \bullet \left(\frac{L}{V_{OUT} + V_D - V_{IN}} \right) \quad \text{.....} \quad (9)$$

Since I_L=0 at time t_{OFF} (when all inductor energy was emitted), the following is obtained from equation (7):

$$\frac{L}{V_{OUT} + V_D - V_{IN}} = \frac{t_{OFF}}{I_{PK}} \quad \text{.....} \quad (10)$$

The following is obtained by substituting equation (10) into equation (9):

$$t_1 = t_{OFF} - \left(\frac{I_{OUT}}{I_{PK}} \right) \bullet t_{OFF} \quad \text{.....} \quad (11)$$

The amount of electric charge ΔQ_1 charged in C_{OUT} during time t_1:

$$\Delta Q_1 = \int_0^{t1} I_L \, dt = I_{PK} \bullet \int_0^{t1} dt - \frac{V_{OUT} + V_D - V_{IN}}{L} \bullet \int_0^{t1} t \, dt$$

$$= I_{PK} \bullet t_1 - \frac{V_{OUT} + V_D - V_{IN}}{L} \bullet \frac{1}{2} t_1^2 \quad \text{.....} \quad (12)$$

The following is obtained by substituting equation (9) into equation (12)

$$\Delta Q_1 = \left[I_{PK} - \frac{1}{2} (I_{PK} - I_{OUT}) \right] \bullet t_1 = \left(\frac{I_{PK} + I_{OUT}}{2} \right) \bullet t_1 \quad \text{.....} \quad (13)$$

The voltage rise (V_{P-P}) due to ΔQ_1 is as follows:

$$V_{P-P} = \frac{\Delta Q_1}{C_{OUT}} = \frac{1}{C_{OUT}} \bullet \left(\frac{I_{PK} + I_{OUT}}{2} \right) \bullet t_1 \quad \text{.....} \quad (14)$$

The following is obtained when the I_{OUT} consumed during time t_1 and R_{ESR}, which is the Electric Series Resistance (ESR) of C_{OUT}, are taken into consideration:

$$V_{P-P} = \frac{\Delta Q_1}{C_{OUT}} = \frac{1}{C_{OUT}} \bullet \left(\frac{I_{PK} + I_{OUT}}{2} \right) \bullet t_1 + \left(\frac{I_{PK} + I_{OUT}}{2} \right) \bullet R_{ESR} - \frac{I_{OUT} \bullet t_1}{C_{OUT}} \quad \text{.....} \quad (15)$$

The following is obtained when equation (11) is substituted into equation (15):

$$V_{P-P} = \frac{(I_{PK} - I_{OUT})^2}{2 I_{PK}} \bullet \frac{t_{OFF}}{C_{OUT}} + \left(\frac{I_{PK} + I_{OUT}}{2} \right) \bullet R_{ESR} \quad \text{.....} \quad (16)$$

Effective ways to reduce the ripple voltage are to increase the capacitance of the capacitor connected to the output pin and to reduce its ESR.

Note:

Although this IC has an on-chip soft-start circuit, a rush current flows because the output capacitor (C_{OUT}) and load capacitance component are charged up via the coil and diode on power application. Therefore, care must be taken.

3. Inverter type switching regulator (DC/DC Q)

The fundamental equations of the inverter type regulator are shown below.

Point A voltage immediately after M1 is turned on (I_L, which is the current that flows to L, is zero):

$$V_A = V_{IN} - V_S \quad \text{.....} \quad (17)$$

(V_S: Unsaturated voltage of M1)

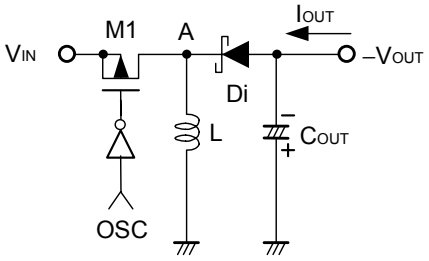


Figure 5 Inverter Type Switching Regulator

Change in I_L with time:

$$\frac{dI_L}{dt} = \frac{V_L}{L} = \frac{V_{IN} - V_S}{L} \quad \text{.....} \quad (18)$$

Result of integrating the above equation (I_L):

$$I_L = \left(\frac{V_{IN} - V_S}{L}\right) \bullet t \quad \text{.....} \quad (19)$$

The current I_L flows during time t_{ON}. This time (t_{ON}) is determined according to the oscillation frequency of OSC.

Peak current (I_{PK}) after t_{ON}:

$$I_{PK} = \left(\frac{V_{IN} - V_S}{L}\right) \bullet t_{ON} \quad \text{.....} \quad (20)$$

The energy stored in L at this time is represented by $1/2 \cdot L(I_{PK})^2$.

Next, when M1 is turned off, the energy stored in L is emitted through ground→capacitor→diode (Di), and a counter voltage (V_L) is generated at the same time.

V_L:

$$V_L = -(V_{OUT} + V_D) \quad \text{.....} \quad (21)$$

(V_D: Diode forward voltage)

Change with time of current (I_L) that flows to $-V_{OUT}$ through a capacitor during time t_{OFF}:

$$\frac{dI_L}{dt} = \frac{V_L}{L} = \frac{V_{OUT} + V_D}{L} \quad \text{.....} \quad (22)$$

Result of integrating the above equation:

$$I_L = I_{PK} - \left(\frac{V_{OUT} + V_D}{L}\right) \bullet t \quad \text{.....} \quad (23)$$

During t_{ON}, the energy is stored in L and not transmitted to $-V_{OUT}$. When output current (I_{OUT}) flows from $-V_{OUT}$, the capacitor (C_{OUT}) energy is used. As a result, the C_{OUT} pin voltage decreases and reaches its lowest value after time t_{ON}. When M1 is turned off, the energy stored in L is transmitted through the diode to C_{OUT}, and the C_{OUT} pin voltage rises dramatically. V_{OUT} is a time function that indicates the maximum value (ripple voltage: V_{P-P}) when the current flowing through the diode to V_{OUT} matches the load current I_{OUT}.

This ripple voltage value is calculated below.

I_{OUT} when the time from immediately after t_{ON} until V_{OUT} reaches its highest level is set to t_1:

$$I_{OUT} = I_{PK} - \left(\frac{V_{OUT} + V_D}{L} \right) \bullet t_1 \quad \text{..... (24)}$$

$$\therefore t_1 = (I_{PK} - I_{OUT}) \bullet \left(\frac{L}{V_{OUT} + V_D} \right) \quad \text{..... (25)}$$

Since I_L=0 at time t_{OFF} (when all inductor energy was emitted), the following is obtained from equation (23):

$$\frac{L}{V_{OUT} + V_D} = \frac{t_{OFF}}{I_{PK}} \quad \text{..... (26)}$$

The following is obtained by substituting equation (26) into equation (25):

$$t_1 = t_{OFF} - \left(\frac{I_{OUT}}{I_{PK}} \right) \bullet t_{OFF} \quad \text{..... (27)}$$

The amount of electric charge ΔQ_1 charged in C_{OUT} during time t_1:

$$\Delta Q_1 = \int_0^{t1} I_{OUT}\, dt = I_{PK} \bullet \int_0^{t1} dt - \frac{V_{OUT} + V_D}{L} \bullet \int_0^{t1} t\, dt$$

$$= I_{PK} \bullet t_1 - \frac{V_{OUT} + V_D}{L} \bullet \frac{1}{2} t_1^2 \quad \text{..... (28)}$$

The following is obtained by substituting equation (25) into equation (28)

$$\Delta Q_1 = I_{PK} - \frac{1}{2}(I_{PK} - I_{OUT}) \bullet t_1 = \frac{I_{PK} + I_{OUT}}{2} \bullet t_1 \quad \text{..... (29)}$$

The voltage rise (V_{P-P}) due to ΔQ_1 is as follows:

$$V_{P-P} = \frac{\Delta Q_1}{C_{OUT}} = \frac{1}{C_{OUT}} \bullet \left(\frac{I_{PK} + I_{OUT}}{2} \right) \bullet t_1 \quad \text{..... (30)}$$

The following is obtained when the I_{OUT} consumed during time t_1 is taken into consideration:

$$V_{P\text{-}P} = \frac{\Delta Q_1}{C_{OUT}} = \frac{1}{C_{OUT}} \bullet \left(\frac{I_{PK} + I_{OUT}}{2} \right) \bullet t_1 - \frac{I_{OUT} \bullet t_1}{C_{OUT}} \quad \text{..... (31)}$$

The following is obtained when equation (27) is substituted into equation (31):

$$V_{P\text{-}P} = \frac{(I_{PK} - I_{OUT})^2}{2I_{PK}} \bullet \frac{t_{OFF}}{C_{OUT}} \quad \text{..... (32)}$$

■ Operation Modes and Mode Control

The mode is switched among modes 1 to 3 according to the 2-bit input from the MC1 and MC2 pins and the MC3 signal. The MC3 signal is not an input to a pin of this IC. It is a signal required for external part control. This signal should be supplied from the LCD driver or LCD controller.

Since the MC1 and MC2 pins are not pulled up or pulled down internally, they should not be in a floating state. Also, note that the current consumption in standby mode may exceed 1 μA if there is a potential difference between the supply voltage of MC1 and MC2 and the supply voltage of the S-8335 Series IC.

MC1	MC2	MC3*	Operation Mode
L	L	H	Mode 1 (Normal operation)
L	H	L	Mode 2 (Icon mode)
H	X	L	Mode 3 (Standby mode)

Remark: L: Low level, H: High level, X: Don't care

* MC3 is a signal that is the input to an external switch to forcibly discharge a capacitor in modes 2 and 3.

1. Normal operation mode (MC1=L, MC2=L, MC3=H)

   Step-up operation is performed.

2. Icon mode (MC1=L, MC2=H, MC3=L)

   Only the reference voltage circuit and regulator S operate. The regulator S output V_{REGSO} can be set arbitrarily in the range from 1.0 to 2.2 V by using external resistors RS1 and RS2. V_{REGSO} can be used as the icon voltage. Use an RS1 value that matches the temperature characteristics of the panel by combining a series or parallel resistor with a thermistor as necessary. See the section on regulator S for information about the output voltage characteristics of regulator S when the output current is drawn.

3. Standby mode (MC1=H, MC3=L)

   The operation of internal circuits is shut down. The current consumption does not exceed 1 μA.

   When the MC1 pin is set high ("H" level), the operation of all internal circuits stops, and the current consumption is dramatically reduced. At the same time, the VOUT1, VXO, VYO, VREGSO, and VREGTO pins are each short-circuited to V_{SS} by on-chip Nch transistors. (However, data that was written to the register of the electric volume part is retained if a voltage of at least 2 V is applied between the VBAT and VSS pins.) Since current flows at this time from the VOUT1 pin to V_{SS} through a coil and a diode at the input side, a switch for shutting down the current is required.

   Figure 6 shows a sample circuit that uses NEC's 2SJ356 (Pch MOSFET) as the current breaker switch. In this sample circuit, the small signal transistor E (Nch MOSFET) is used to turn 2SJ356 on or off by inputting the control signal MC3 to the gate of transistor E.

   An invalid current flowing to resistor RA1 during a step-up operation may affect efficiency. Resistor RA1 should be set to a high resistance value to reduce current. However, if the RA1 resistance value is set too high, a voltage drop across resistor RA1 will occur due to the off-leak current of the small signal transistor E, and the 2SJ356 current breaker switch may not turn off. Therefore, care must be taken.

   Note:

   The efficiency characteristics shown in the reference data, which were measured without a current breaker switch, differ from the efficiency of this sample circuit.

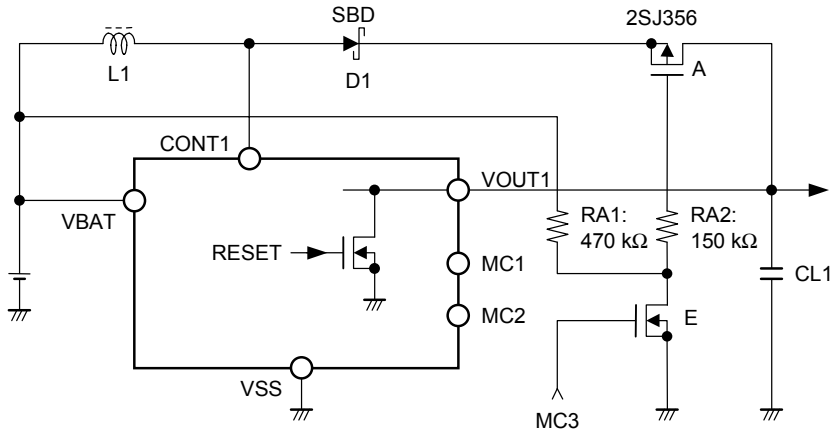


Figure 6 Sample Circuit in Which 2SJ356 is Used

When mode 3 (standby mode) is canceled, the mode returns to the one that was in effect before switching to standby mode. For example, if the IC entered mode 3 from mode 1, it will return to mode 1 when mode 3 is canceled.

Note 1:

If there is a potential difference between the applied voltage to MC1 and MC2 and the power supply voltage of the S-8335 Series, the current consumption in standby mode may exceed 1 µA.

For example, when the applied voltage to MC1 and MC2 is 3.0 V and the power supply voltage of the S-8335 Series is 5.0 V, the current consumption in standby mode rises to approximately 2.5 µA at 25°C (typ.) (see Figure 7). The reason this occurs is that a penetrating current flows in CMOS logic circuits because the potential of input signals MC1 and MC2 (3.0 V) is lower than the internal logic power supply voltage (5.0 V).

Therefore, use this IC in such a way that no potential difference occurs between the applied voltage to MC1 and MC2 and the power supply voltage of the S-8335 Series.

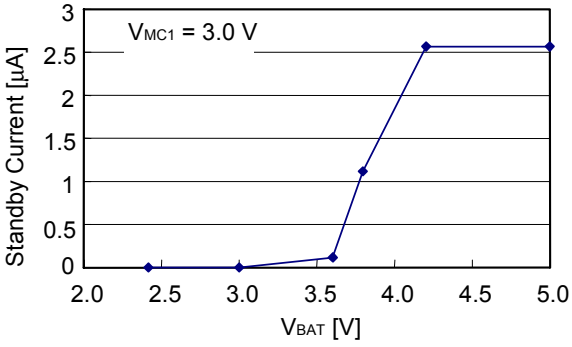


Figure 7 Standby Mode Current Characteristics

Note 2:

A penetrating current from V_{BAT} to V_{SS} flows when the mode is switched. When MC1 (or MC2) = "H" and MC3 = "H", a current of approximately 6 mA flows from the VBAT pin through the coil L1, diode D1, and transistor A because the VOUT1 pin is short-circuited to GND level.

Also, when MC1 (or MC2) = "L" and MC3 = "L", VRL and GND are short-circuited via
transistor G, and a current of approximately 150 mA flows.

To reduce the penetrating current, the MC1 (or MC2) and MC3 signals should both be switched at the same time when modes are switched. If this cannot be done, avoid a state in which the MC1 (or MC2) and MC3 signals are both low ("L" level) at the same time in order to reduce the penetrating current (see Figure 8).

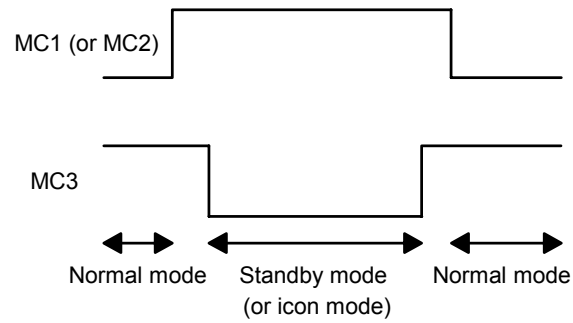


Figure 8 Mode Switching

■ Electric volume

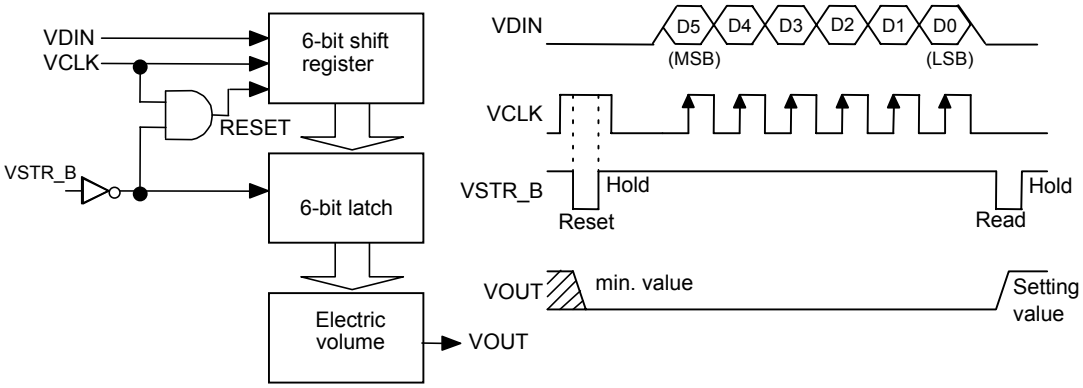


Figure 9 Block Diagram and Clock Timing of Electric Volume Part

VDIN: This is the data input pin to the electric volume.
"Data 1" is an input for the “H” level, and "data 0" is an input for the "L" level.
(A high impedance state is prohibited.) When no data is sent, keep VDIN at the "L" level.

VCLK: This is the clock input pin to the electric volume.
The data of the VDIN pin is fetched to the shift register at the clock rising edge. When a clock with more than six bits data is input, the data that had been read is sequentially shifted at each clock pulse, and the last six bits of data become effective.

VSTR_B: This is the strobe signal input pin.
When the strobe signal goes low (set to "L" level), the shift register contents are fetched to the latch. The data that is fetched to the latch is sent directly to the electric volume, and consequently the output voltage changes. When the strobe signal goes high (set to "H" level), the latch data is held.

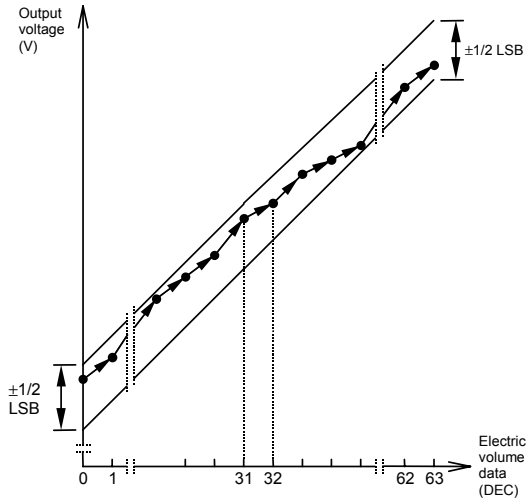


Figure 10 Linearity Error

The electric volume has 6-bit resolution. The integral and differential linearity errors are ±0.5LSB. For example, if you want the VRH output voltage range to vary between 8.91 and 16.59 V, you can obtain a linearity precision of ±61 mV by selecting the S-8335A240FT.

Since the register contents are undefined when the power is turned on, they must be reset. Even if the MC1 pin or MC2 pin is set high ("H" level) and the MC3 signal is set low ("L" level) and the step-up operation stops, the electric volume register contents are retained if a voltage of at least 2 V is applied between the VBAT and VSS pins. Register “WRITE” and “RESET” operations are also available in this state.

The register is initialized to “000000” and the output voltage is set to its minimum value by setting VCLK = "H" and VSTR_B = "L".

Turn on the power with MCI = “H” and MC3 = “L”. Then initialize the register contents by setting VCLK = "H" and VSTR_B="L" and begin the step-up operation by switching the MC1 and MC2 pins low ("L" level) and the MC3 signal high ("H" level).

Caution:

If a step-up operation is started without initializing the data in the register after turning on the power, the maximum output voltage may appear at the VOUT pins and connected devices or instruments may be damaged. It is recommended to connect a pull-down resistor between V_{SS} and the external part pins that the MC3 signal enters and to connect a pull-up resistor between the MC1 pin and V_{BAT}.

Note:

If there is a potential difference between the applied voltage to VDIN, VCLK, and VSTR_B and the power supply voltage of the S-8335 Series, the current consumption in standby mode may exceed 1 μA. For example, when the applied voltage to VDIN, VCLK, and VSTR_B is 3.0 V and the power supply voltage of the S-8335 Series is 5.0 V, the current consumption in standby mode rises to approximately 2.5 μA at 25°C (typ.) (see Figure 11). The reason this occurs is that a penetrating current flows in the CMOS logic circuits because the potential of input signals VDIN, VCLK, and VSTR_B (3.0 V) is lower than the internal logic power supply voltage (5.0 V). A similar situation occurs for the power supply voltage of MC1 and MC2 (see Note in the Mode Control section).

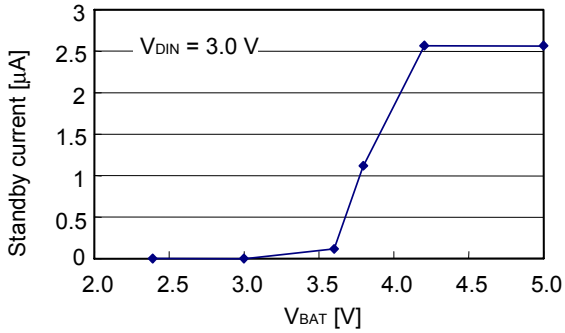


Figure 11 Standby Mode Current Characteristics

■ OP amplifier X

The power supply voltage of OP amplifier X is generated using DC/DC U so that it is approximately 1.05 times larger than the output voltage of OP amplifier X. Since the difference between the power supply voltage and output voltage is kept small, the power loss is extremely small and efficiency is increased. Figure 12 shows the output voltage of OP amplifier X when source current is drawn.

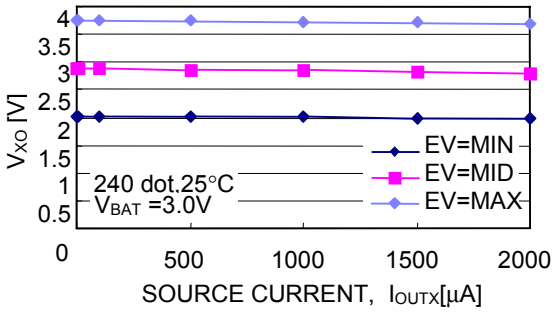


Figure 12 OP Amplifier X Output Voltage

■ OP amplifier Y

V_{BAT} is used for the power supply voltage of OP amplifier Y. Figures 13 and 14 show the output voltage of OP amplifier Y when source current and sink current are drawn, respectively.

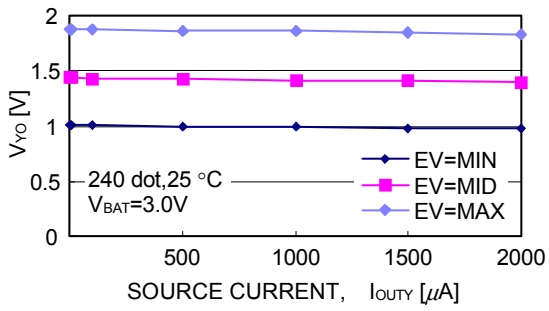


Figure 13 VYO Pin Source Current Characteristics

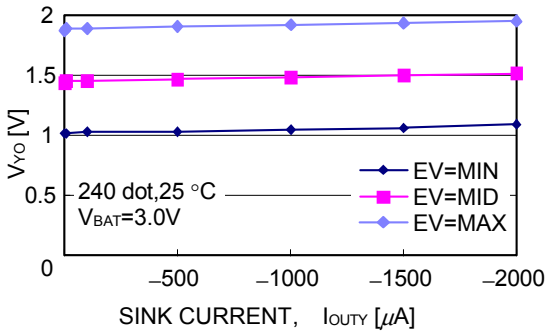


Figure 14 VYO Pin Sink Current Characteristics

■ Regulator S Part

V_{BAT} is used for the power supply voltage of the regulator S part. The regulator S output V_{REGSO} can be set arbitrarily in the range from 1.0 to 2.2 V by using external resistor RS1 and RS2. V_{REGSO} can be used as the icon voltage. Use an RS1 value that matches the temperature characteristics of the panel by combining a series or parallel resistor with a thermistor as necessary.

Also, CRS1 is a capacitor for preventing oscillation. It is required only when the regulator oscillates. Adjust the CRS1 value when the RS1 and RS2 values are changed. Using the actual device, confirm that the regulator does not oscillate. Figure 15 shows the voltage V_{REGSO} when current is drawn.

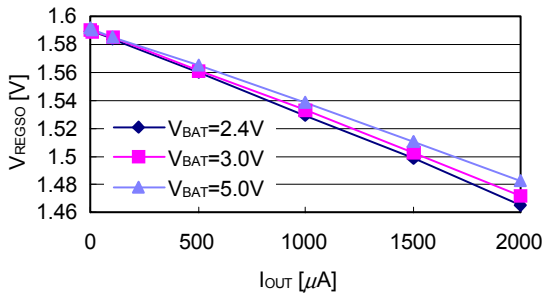


Figure 15 V_{REGSO} Characteristics

■ Regulator T Part

V_{BAT} is used for the power supply voltage of the regulator T part. The regulator T output V_{REGTO} can be set by using external resistance RT1 and RT2. Set V_{REGTO} to match the voltage range that is to be used.

The common-driver voltage V_{RH_max} is obtained by $V_{REGTO} \times 7.136$, and V_{RH_min} is obtained by $V_{REGTO} \times 3.832$. Figure 16 shows the voltage V_{REGTO} when current is drawn.

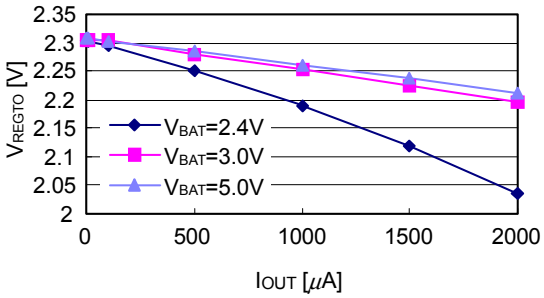


Figure 16 V_{REGTO} Characteristics

■ Power Supply Rising Edge Sequence

The power supply rising edge sequence is V_{RH}, V_{CH}, V_M, V_{RL}. The falling edge sequence is V_{RL}, V_M, V_{CH}, V_{RH}. (See Figure 17.)

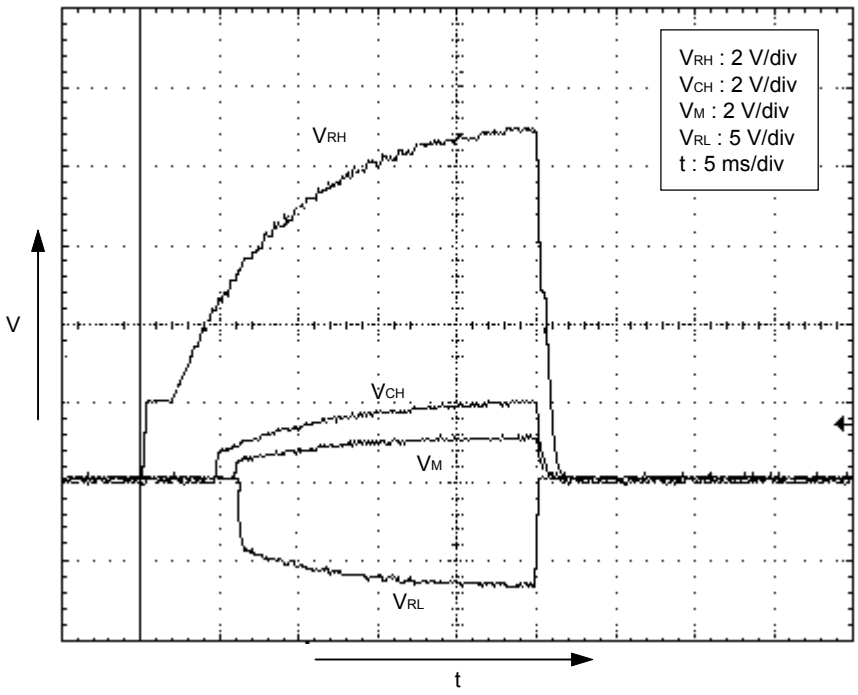


Figure 17 Rising and Falling Edge Sequences

■ Soft Start

The soft-start function blunts the rising edge of the reference voltage V_{REGTO} by using an external capacitor C_{SS} and an internal resistor so that the rush current can be reduced to some degree corresponding to this moderated ascent. However, note that this is not a complete soft start because the switching regulators of the S-8335 Series use PFM control.

■ Selection of External Parts

1. Inductor

The inductance value significantly affects the maximum output current I_{OUT} and efficiency η (EFFI). Figure 18 shows graphs of the dependency of I_{OUT} and EFFI for the S-8335 Series on the inductance value L.

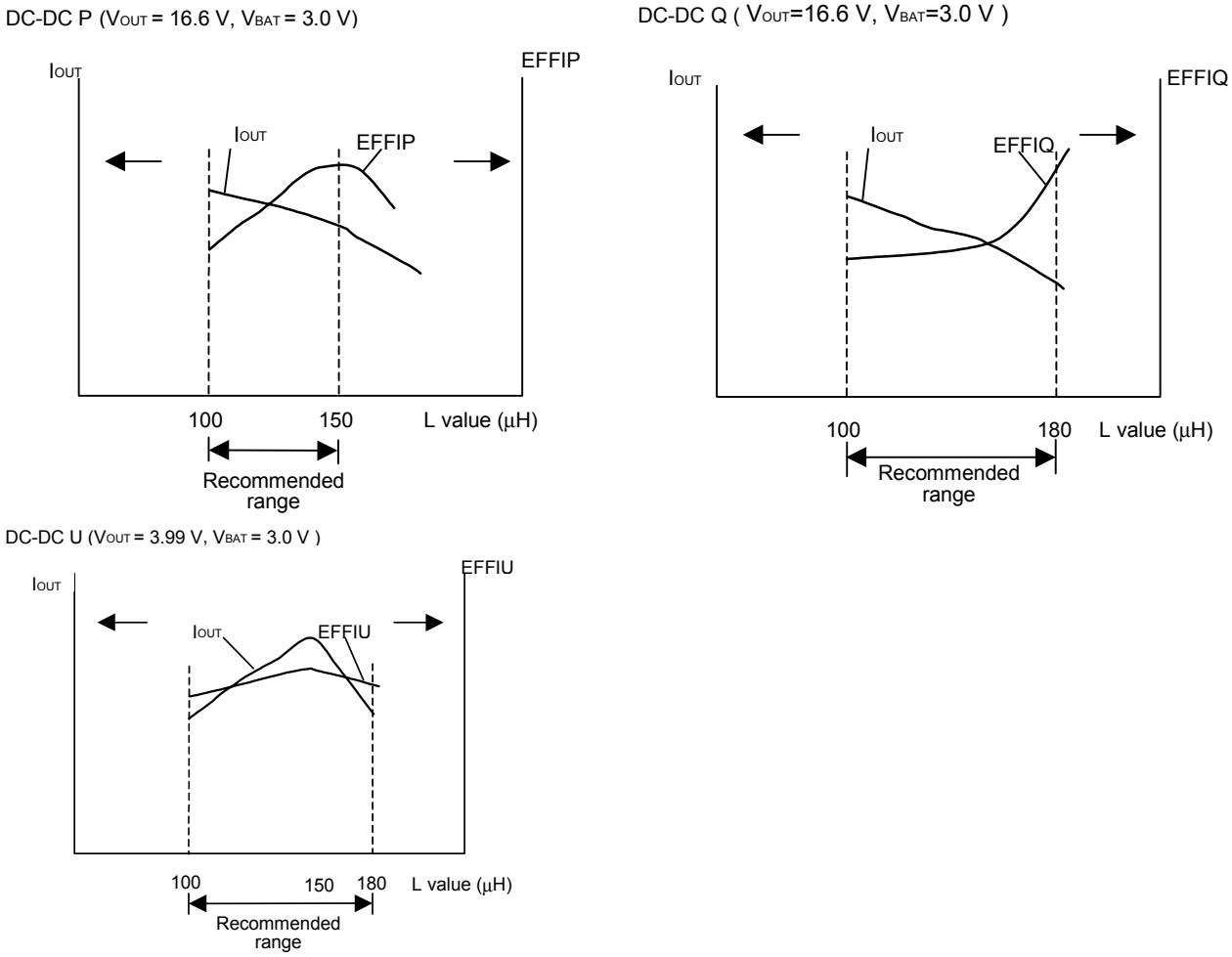


Figure 18 Dependency of I_{OUT} and EFFI on Inductance Value L

As the L value decreases, the peak current I_{PK} increases, and I_{OUT} reaches its maximum at a certain L value. If the L value decreases further, the current driving capability of the switching transistor becomes insufficient, and I_{OUT} is reduced.

Also, as the L value increases, the power loss due to I_{PK} at the switching transistor decreases, and the efficiency reaches its maximum at a certain L value. If the L value increases further, the power loss due to the series resistance of the coil increases, and efficiency is reduced.

The recommended inductance value is 100 to 150 μH for DC/DC P and 100 to 180 μH for DC/DC Q and DC/DC U.

When you select inductors, pay attention to the permissible current of the inductors. If a current that exceeds the permissible current flows in the inductor, magnetic saturation will occur in the inductor. This may cause a significant decrease in efficiency and may damage the IC due to excessive current.

Therefore, select inductors so that the peak current I_{PK} does not exceed the permissible current. The peak current I_{PK} in non-continuous mode is given by the following equation.

$$I_{PK} = \sqrt{\frac{2I_{OUT} \bullet (V_{OUT} + V_D - V_{IN})}{f_{OSC} \bullet L}} \quad (A) \qquad \text{.....} \quad (33)$$

where f_{OSC} is the oscillation frequency. V_D is approximately 0.4 V.

For example, assume that output voltage V_{OUT} = 16.6 V, with load current I_{OUT} = 2mA, using S-8335A240FT with the input voltage V_{IN} = 3 V and f_{OSC} = 100 kHz. If 150 µH is selected for the L value, then I_{PK} = 61 mA from equation (33). Therefore, an inductor having a permissible current of at least 61 mA at an L value of 150 µH should be selected.

2. Diode

An off-chip diode must satisfy the following conditions.

- Low forward voltage: V_F < 0.3 V
- Fast switching speed: 500 ns max.
- Reverse breakdown voltage: $V_{OUT}+V_F$ or more
- Rated current: I_{PK} or more

3. Capacitors (CVBAT, CL)

The input capacitor (CVBAT) can improve efficiency by decreasing the power supply impedance and stabilizing the input current. Select the capacitor value according to the impedance of the power supply used. Connect a capacitor of at least 1 µF to each of the two power supply pins.

For the output capacitor (CL), use a capacitor having a small Electric Series Resistance (ESR) and large capacitance to stabilize the ripple voltage. Standard capacitor values are at least 2.2 µF for CL1 and CL2 and at least 10 µF for CL3. In particular, a tantalum electrolytic capacitor having excellent low temperature characteristics and low leakage current characteristics should be used. A capacitor having a large capacitance produces more stable output and leads to higher efficiency.

■ Standard Circuits

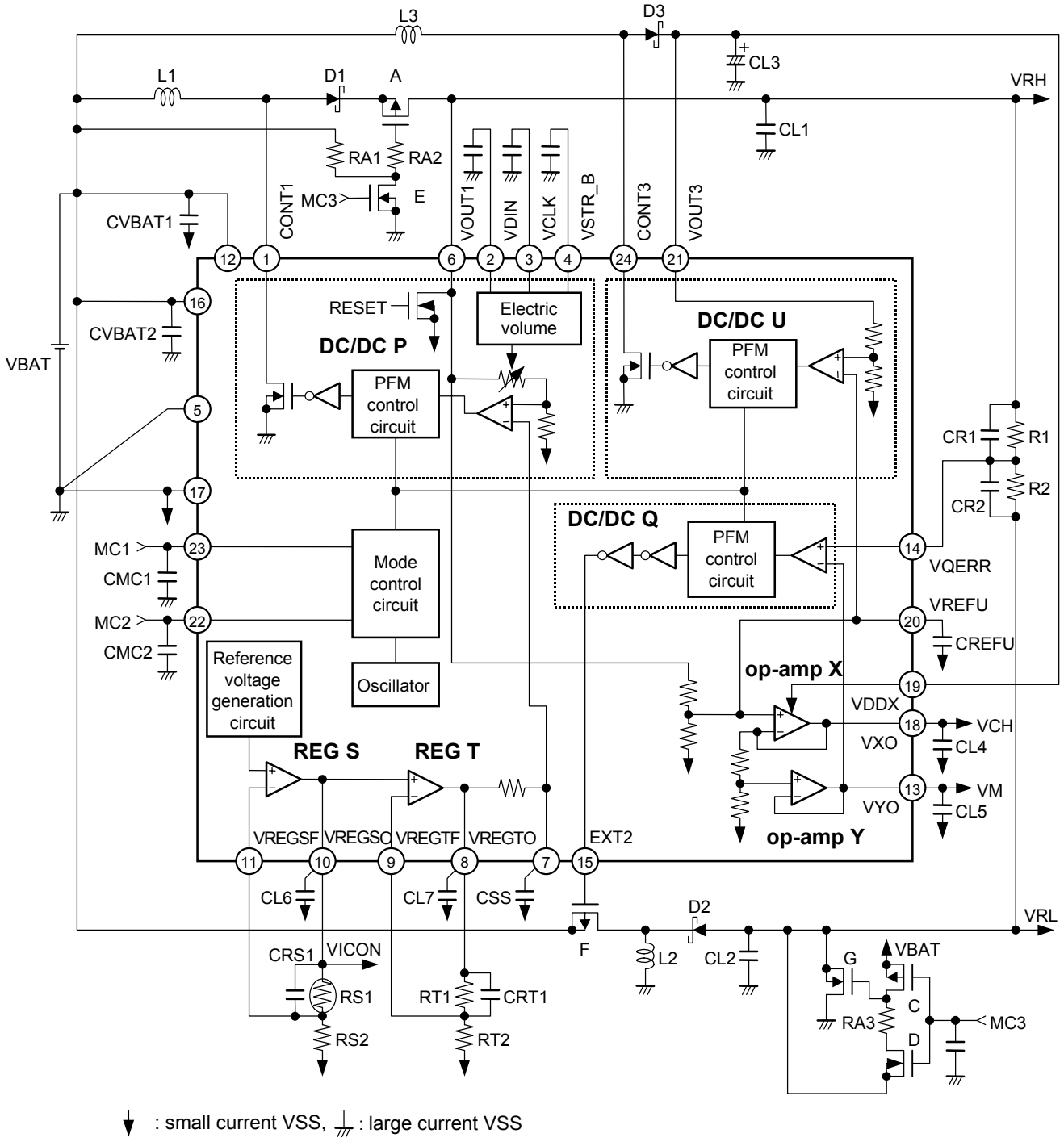


Figure 19 Standard Circuits

Except for op-amp X, all of the power for the internal circuits of the S-8335 Series is supplied by the VBAT pin.

■ Pattern Diagram

In general, the switching regulator is significantly affected by the circuit board wiring. The following figure shows a sample pattern diagram for which the effect of the circuit board wiring is small.

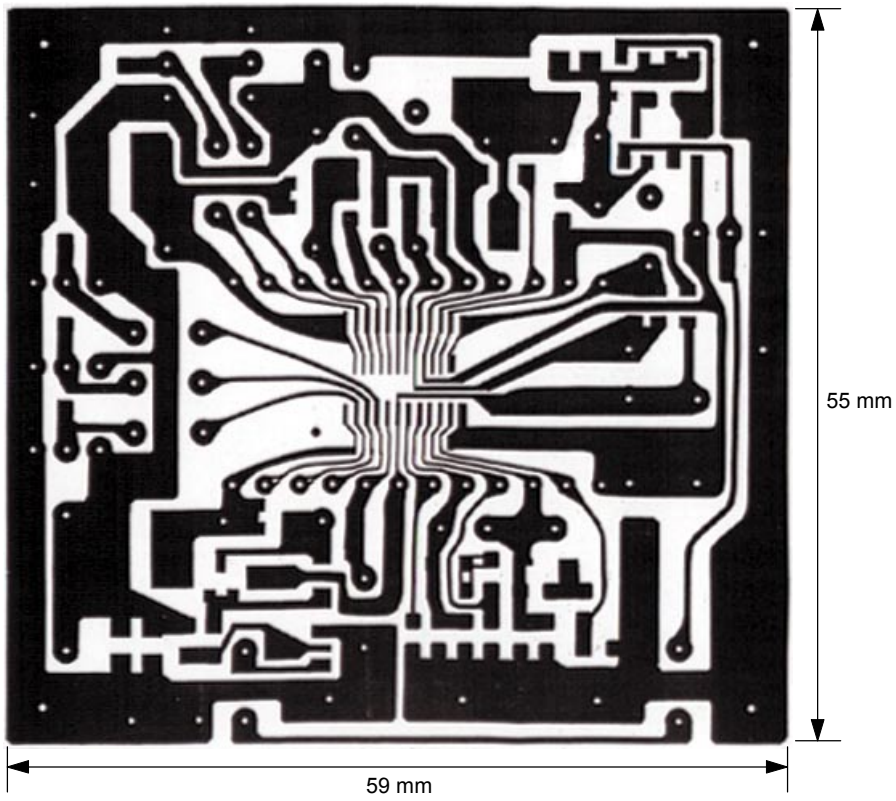


Figure 20 Pattern Diagram

Note the following points when creating a pattern diagram.

- There are two VSS lines (connected inside the IC).
  a) VSS (pin No. 5): Large current GND
  b) VSS (pin No. 17): Small current (analog) + middle current GND
- Arrange the VSS line and capacitors first. CVBAT, CL1, CL2, and CL3 are particularly important. Draw the VSS line as wide as possible.
- Basically, make the GND part of the circuit board as broad as possible and keep the impedance low.
- There are two VBAT lines (not connected inside the IC).
  a) VBAT (pin No. 12): Reference (low noise)
  b) VBAT (pin No. 16): All others (semi-low noise)
- Connect CL3 at both pin No. 19 (VDDX) and pin No. 21 (VOUT3) if possible (for example, connect 6.8 μF at each pin).
- Do not use through holes at locations for connecting CL1 to CL3.
- Increasing CL1 makes the output more stable. If the DC/DC P output fluctuates due to ripple, and this causes VQERR to frequently exceed the DC/DC Q error amplifier threshold value, then DC/DC Q oscillates more than necessary and the DC/DC Q efficiency will decrease. Therefore, stabilizing the DC/DC P output will also improve DC/DC Q efficiency.

■ Application Circuit

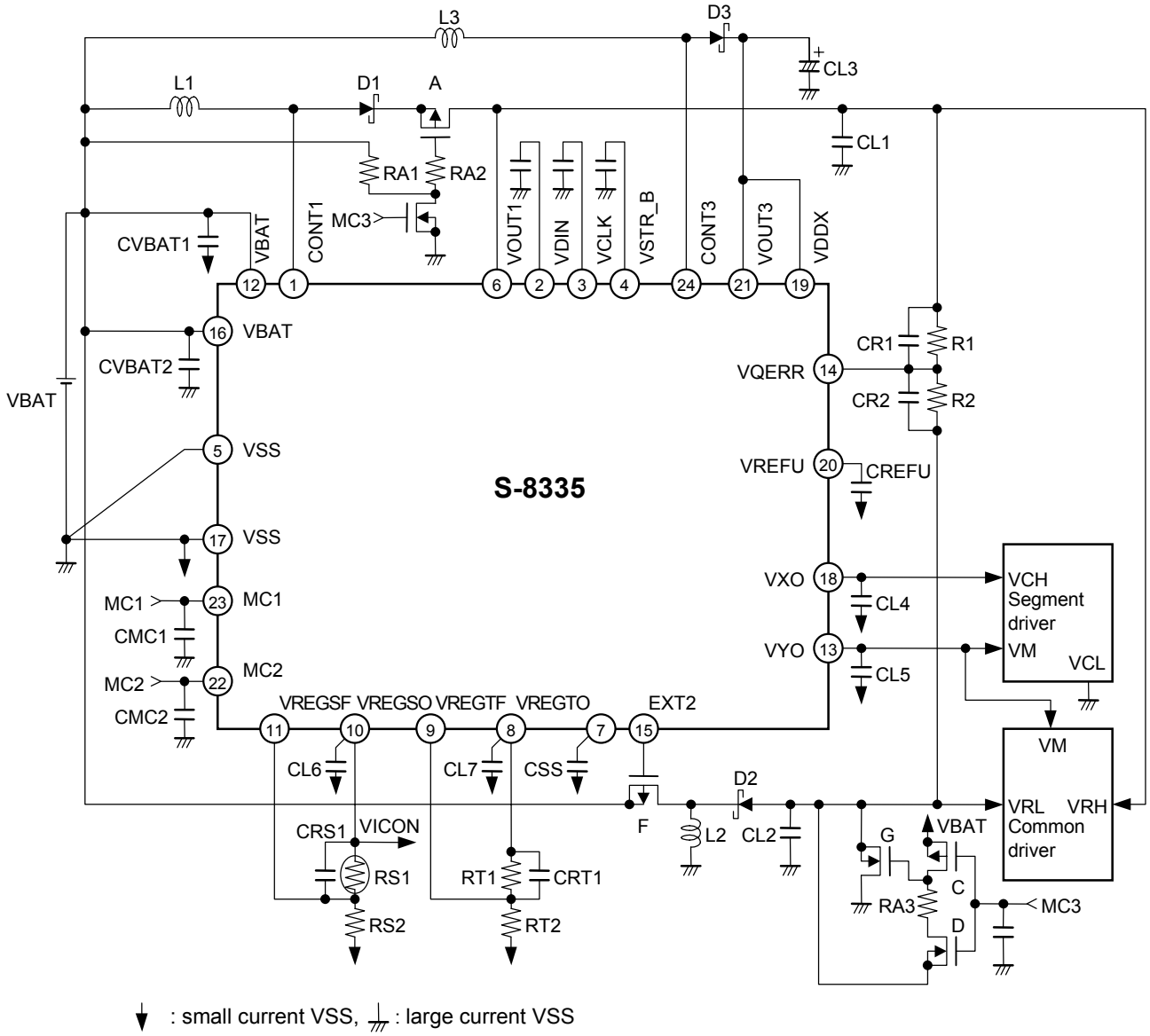


Figure 21 Application Circuit Example

■ Precautions

- Mount external capacitors, diodes, coils, and other components as close as possible to the IC.
- The RS1, RS2, RT1, and RT2 values of the recommended peripheral parts are for V_{ICON} = 1.6 V. If a V_{ICON} value other than 1.6 V is used, the resistance values should be changed. The output voltage precision does not include external resistance dispersion.
- Characteristic ripple voltage and spike noise occur at the switching regulator. Since these are significantly affected by the coil and capacitor that are used, evaluate them using actual devices when the circuit is designed.
- CR1 and CR2 contribute to the stability of the VQERR pin potential and increase the efficiency of switching regulator Q. Although a capacitance value in the range from 1000 pF to 0.01 μF is recommended for CR1 and CR2, you should evaluate this value using an actual device.
- Make sure that the operating ambient temperature range of this IC is not exceeded due to switching transistor power dissipation (particularly at high temperature).

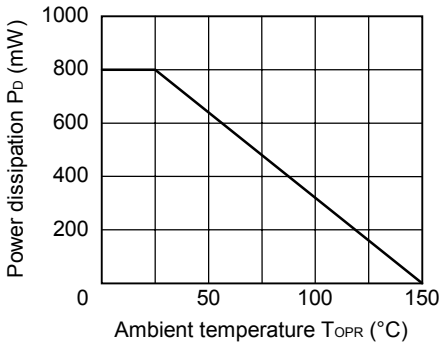


Figure 22 Power Dissipation of 24-pin TSSOP Package (Unmounted)

- Arrange parts so that the line to the VSS pin (indicated by the bold line in Figure 23) is as short as possible. If this line has resistance and inductance components, the VSS potential of the IC will fluctuate due to the switching current. If a potential difference is produced between the VSS of the CPU and the VSS of the IC, a malfunction may occur in the interface, and the electric volume may be reset.

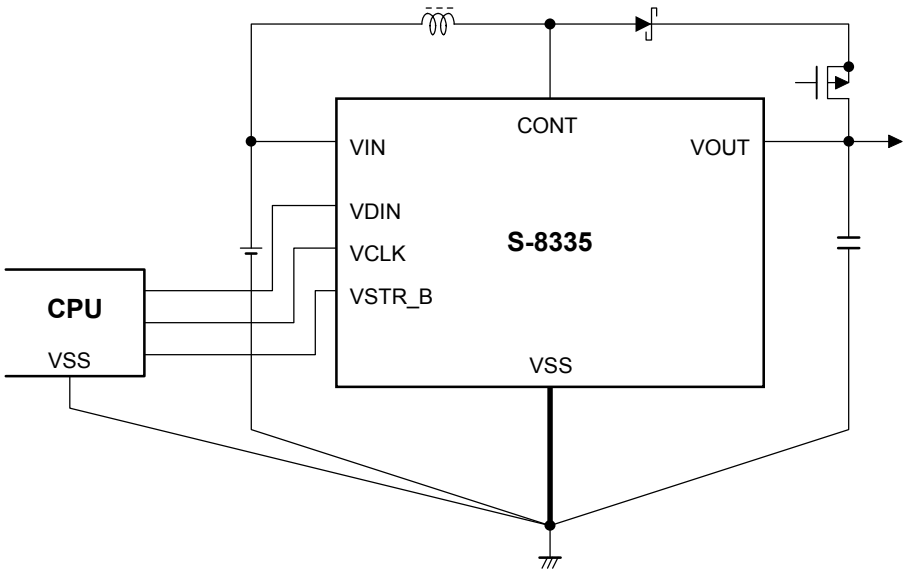


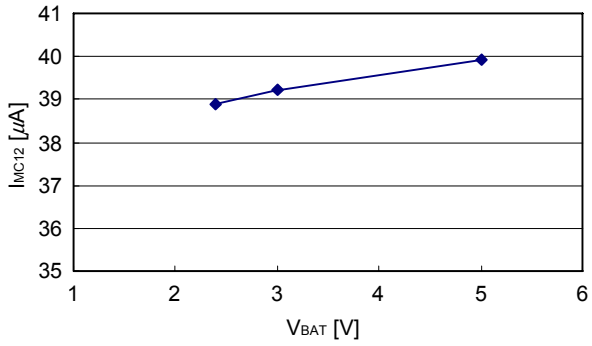
Figure 23 VSS Line

- When switching the output voltage by the electric volume, the soft start does not function. Note that an overshoot will occur when the output voltage increases by a large amount.
- When the internal impedance of the power supply (VBAT) is large, the S-8335 Series may not start up. Make sure that the internal impedance of the power supply used is sufficiently small when using this IC.
- Make sure that the potential of the VOUT1 pin does not exceed 20 V, which is the absolute maximum rating, when using this IC.
- Make the capacitance of VDIN, VCLK, and VSTR_B large enough to prevent noise and malfunctions.
- Seiko Instruments Inc. shall bear no responsibility for any patent infringement by a product that includes an IC manufactured by Seiko Instruments Inc. in relation to the method of using this IC in that product, the product specifications, or the destination country.

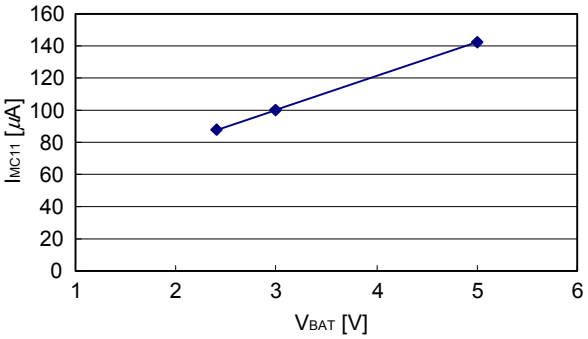
■ Characteristic Curves

1. Common characteristics (Unless otherwise specified, these graphs show typical data for T_{OPR} = 25°C.)

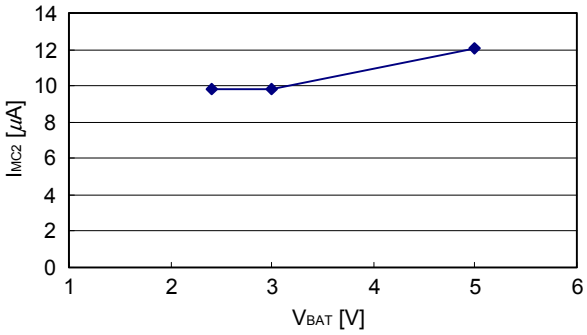
Current consumption
(for mode 1 when oscillation is stopped)



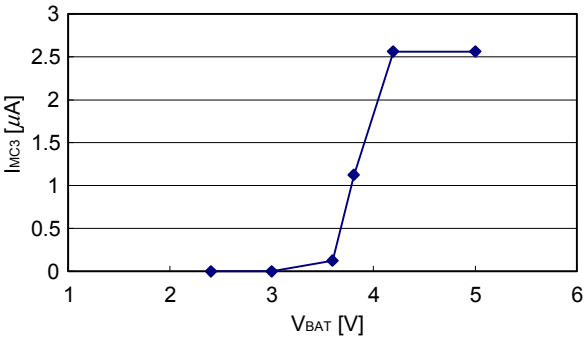
Current consumption
(for mode 1 with full oscillation)



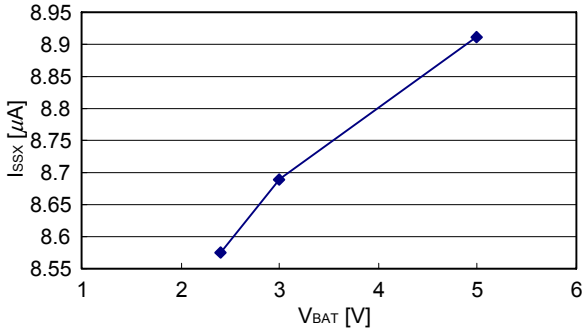
Current consumption (mode 2)



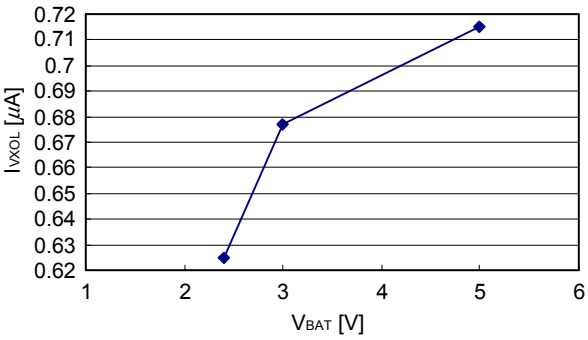
Current consumption (mode 3)



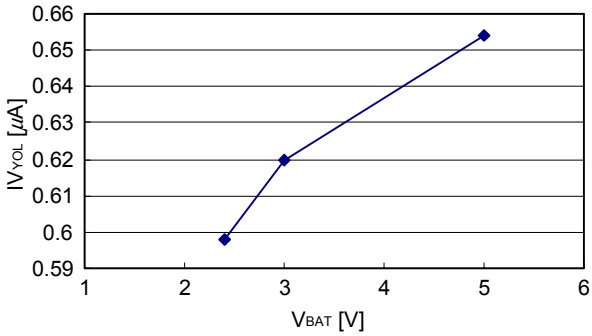
OP amplifier X part current consumption



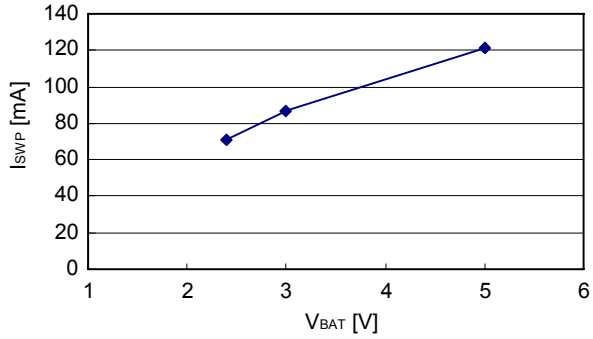
VXO pin sink current



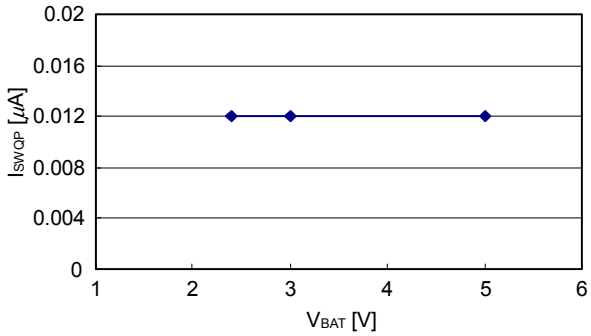
VYO pin sink current



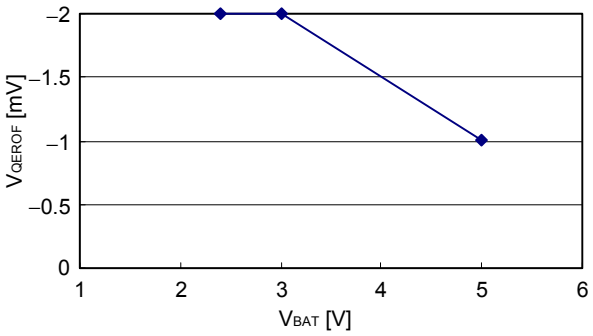
DC/DC P part switching current



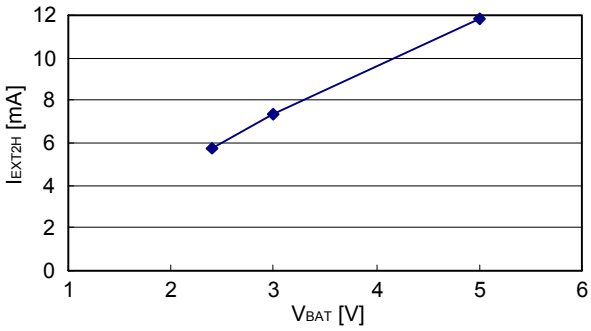
DC/DC P part switching transistor leakage current



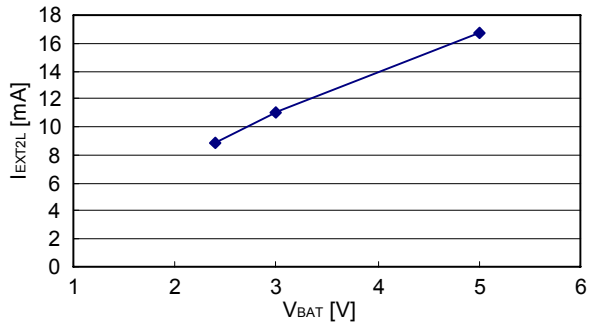
DC/DC Q part comparator offset voltage



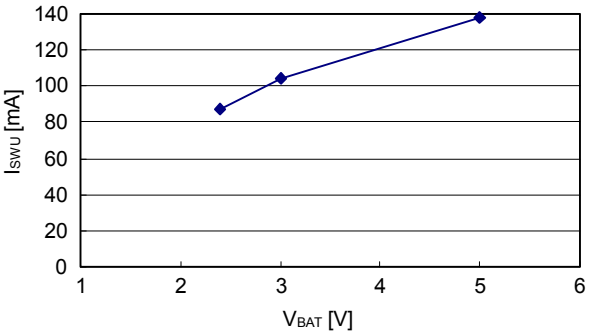
EXT2 pin current (I_{EXT2H})



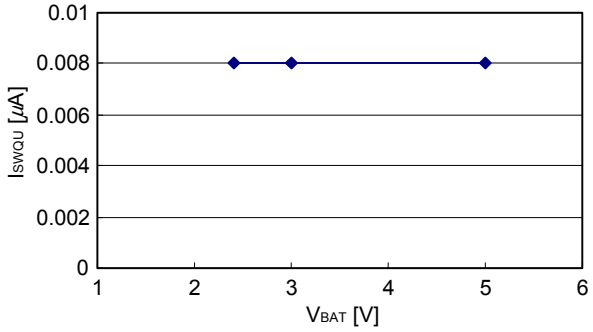
EXT2 pin current (I_{EXT2L})



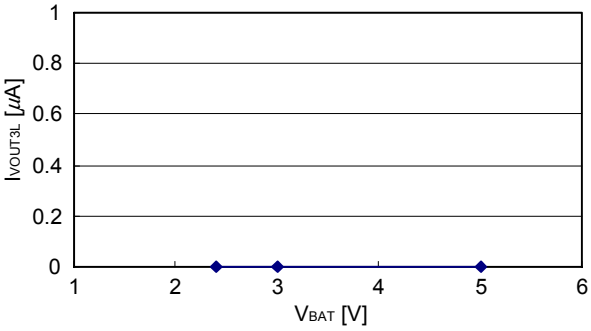
DC/DC U part switching current



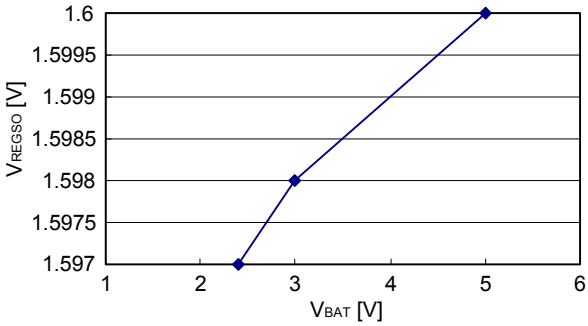
DC/DC U part switching transistor leakage current



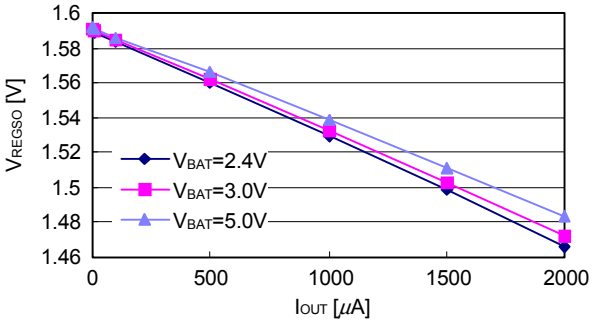
VOUT3 pin off current



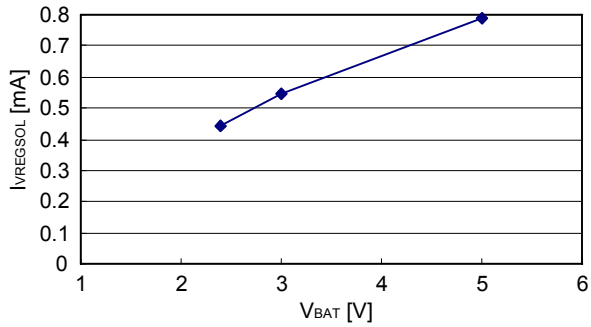
Regulator S part output voltage (vs. V_{BAT})



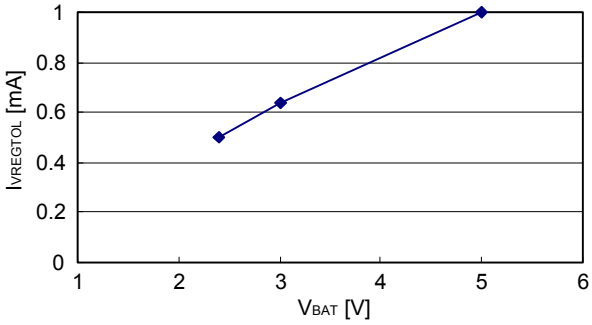
Regulator S part output voltage (vs. I_{OUT})



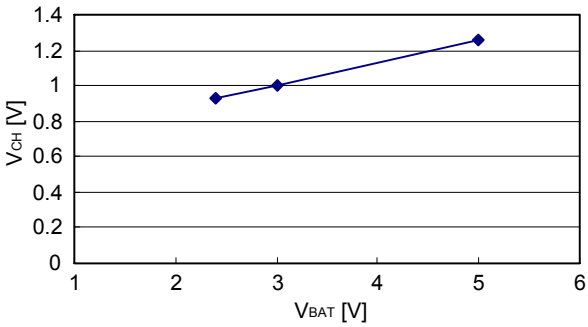
VREGSO pin sink current



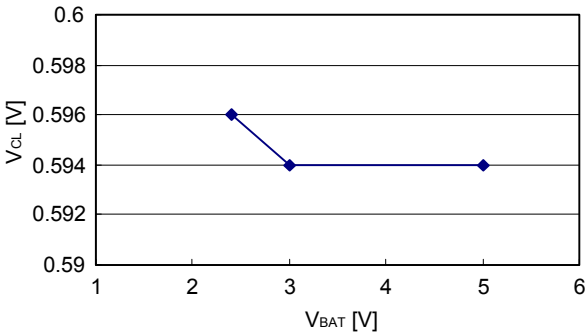
VREGTO pin sink current



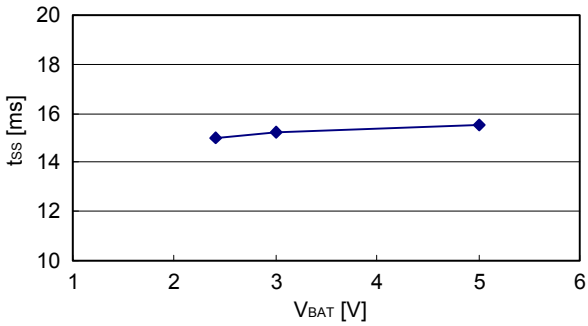
MC1, MC2 pin high level voltage



MC1, MC2 pin low level voltage

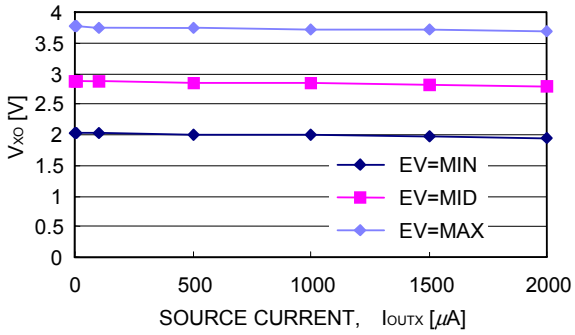


Soft start time

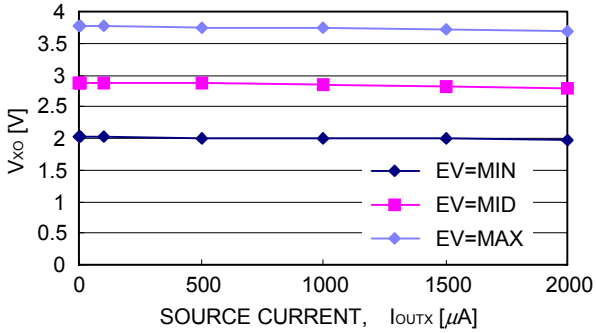


2. S-8335A240FT (1/240 duty. Unless otherwise specified, these graphs show typical data for T_{OPR} = 25°C.)

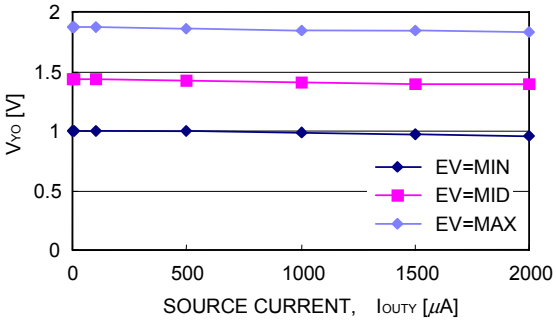
OP amplifier X part output voltage (V_{BAT} = 2.4 V)



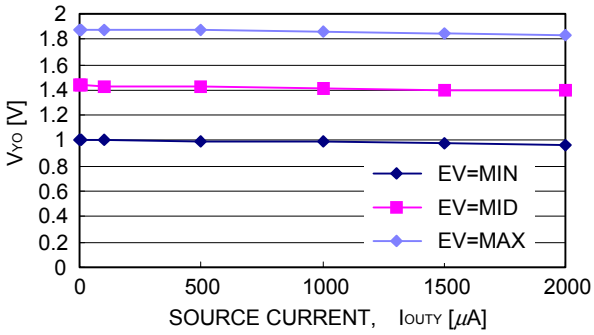
OP amplifier X part output voltage (V_{BAT} = 3.0 V)



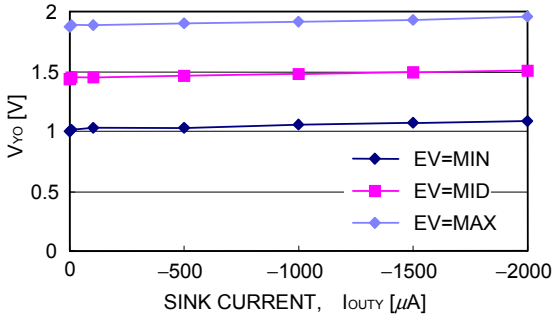
OP amplifier Y part output voltage
(vs. source current, V_{BAT} = 2.4 V)



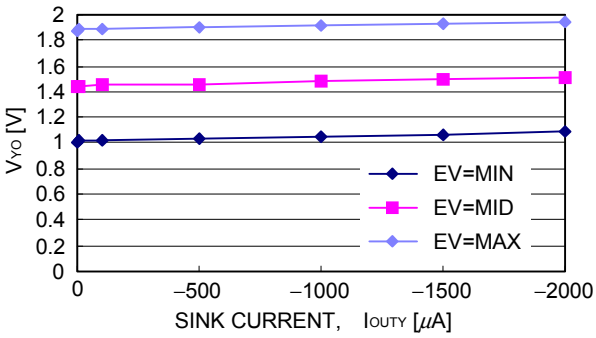
OP amplifier Y part output voltage
(vs. source current, V_{BAT} = 3.0 V)



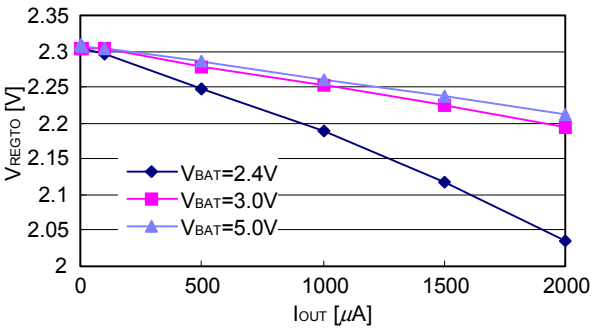
OP amplifier Y part output voltage
(vs. sink current, V_{BAT} = 2.4 V)



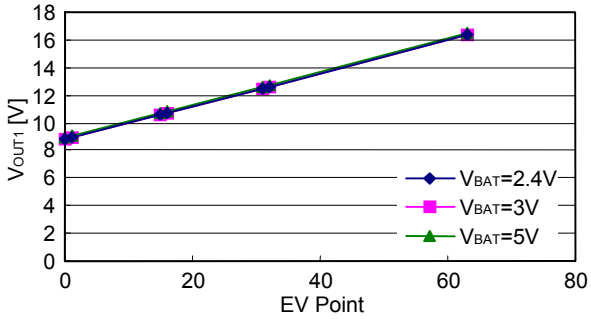
OP amplifier Y part output voltage
(vs. sink current, V_{BAT} = 3.0 V)



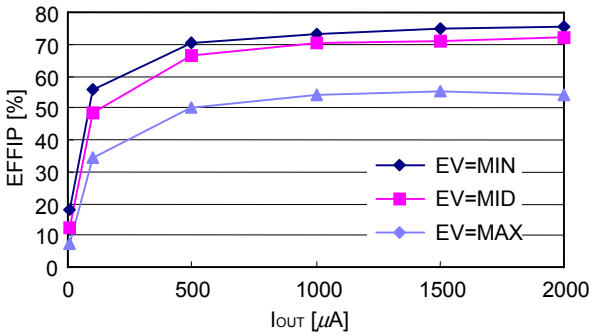
Regulator T part output voltage



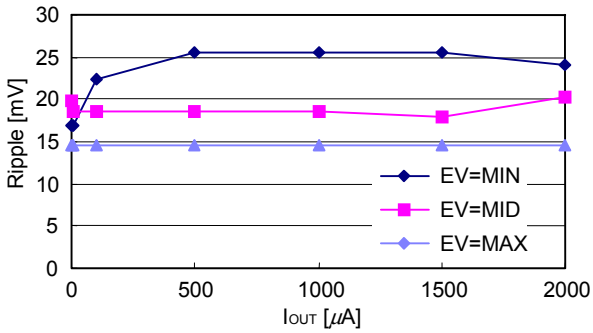
DC/DC P part output voltage



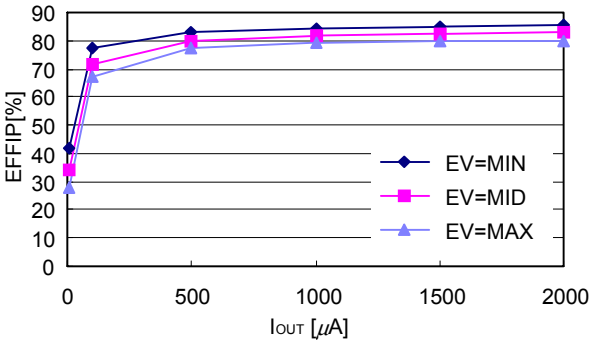
DC/DC P part output efficiency (V_{BAT} = 2.4 V)



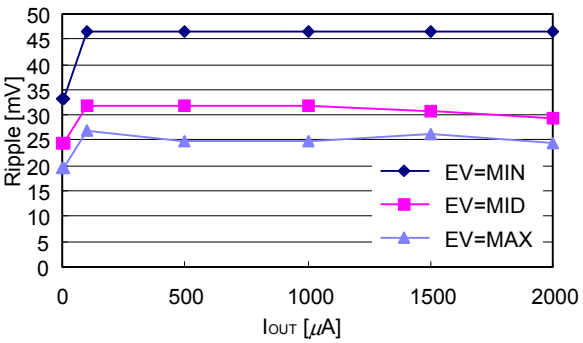
DC/DC P part output ripple voltage (V_{BAT} = 2.4 V, reference value)



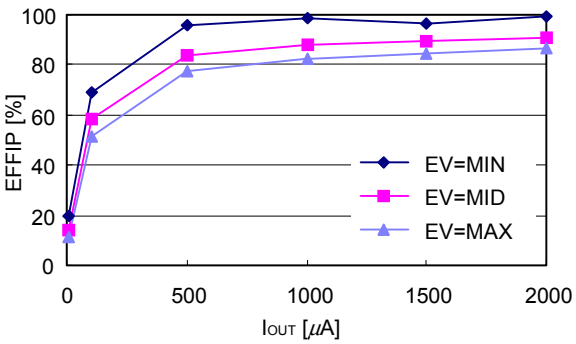
DC/DC P part output efficiency (V_{BAT} = 3.0 V)



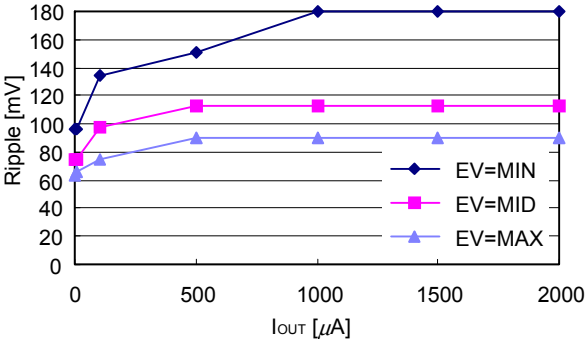
DC/DC P part output ripple voltage (V_{BAT} = 3.0 V, reference value)



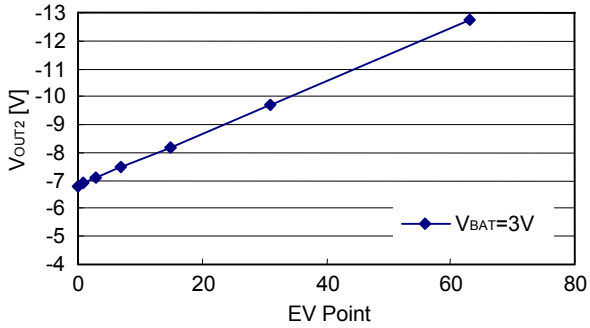
DC/DC P part output efficiency (V_{BAT} = 5.0 V)



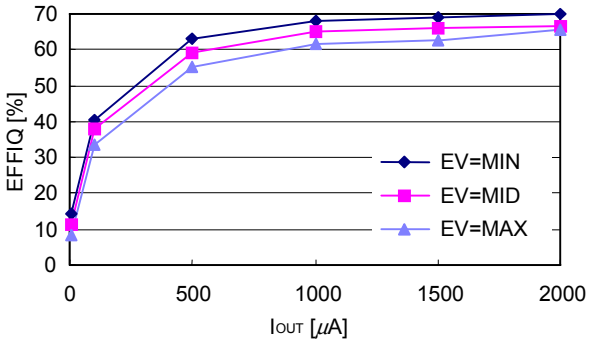
DC/DC P part output ripple voltage (V_{BAT} = 5.0 V, reference value)



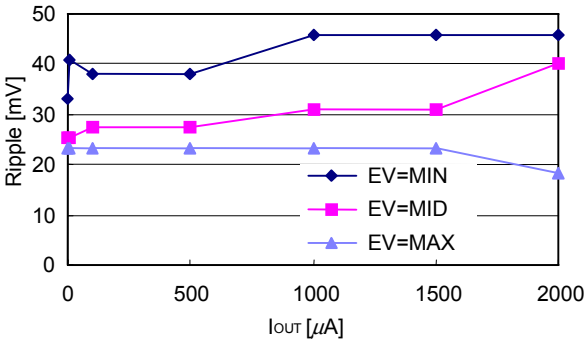
DC/DC Q part output voltage



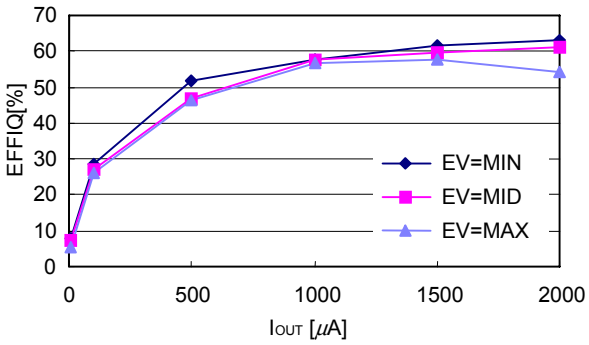
DC/DC Q part output efficiency (V_{BAT} = 2.4 V)



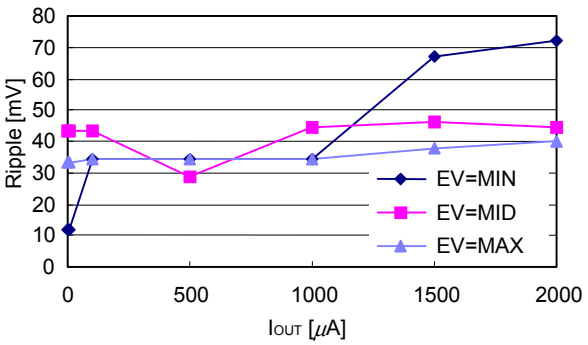
DC/DC Q part output ripple voltage
(V_{BAT} = 2.4 V, reference value)



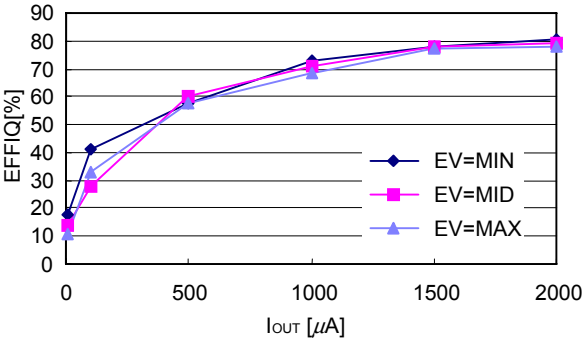
DC/DC Q part output efficiency (V_{BAT} = 3.0 V)



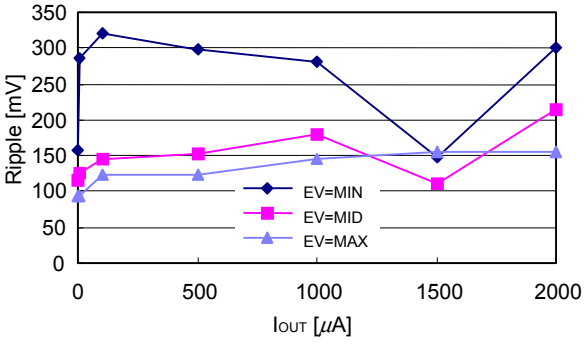
DC/DC Q part output ripple voltage
(V_{BAT} = 3.0 V, reference value)



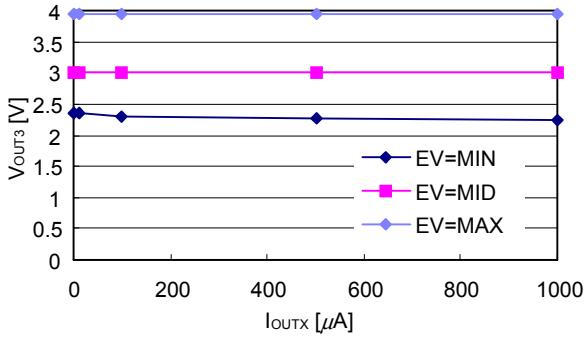
DC/DC Q part output efficiency (V_{BAT} = 5.0 V)



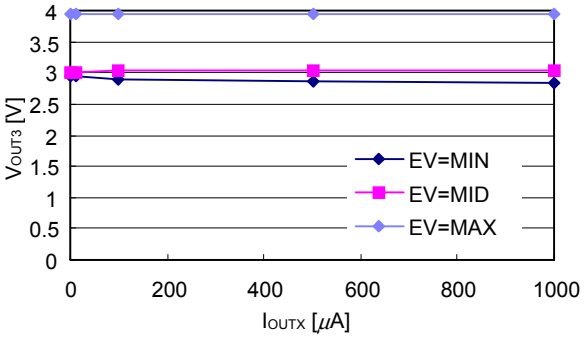
DC/DC Q part output ripple voltage
(V_{BAT} = 5.0 V, reference value)



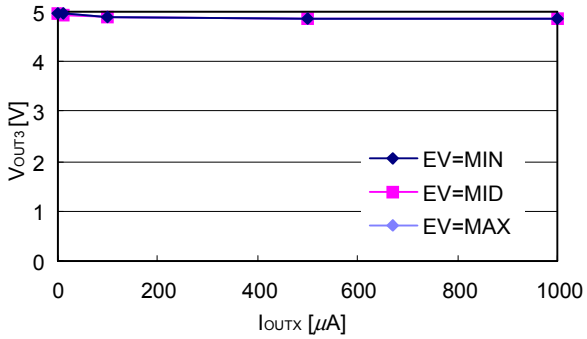
DC/DC U part output voltage (V_{BAT} = 2.4 V)



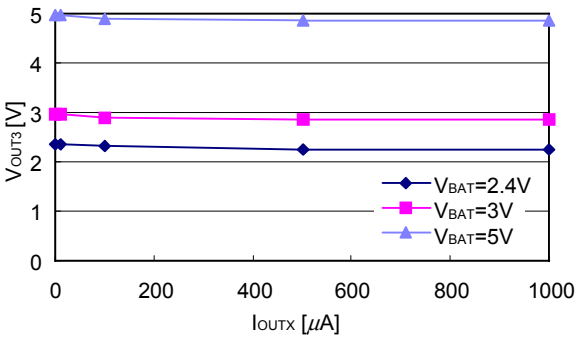
DC/DC U part output voltage (V_{BAT} = 3.0 V)



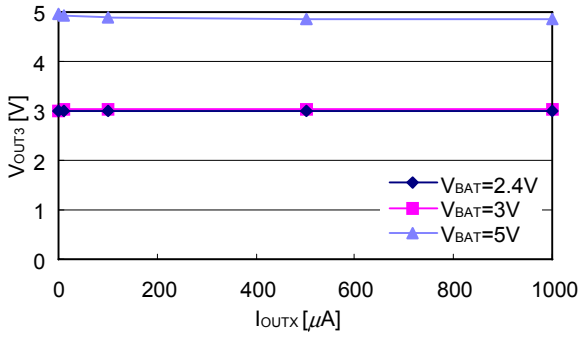
DC/DC U part output voltage (V_{BAT} = 5.0 V)



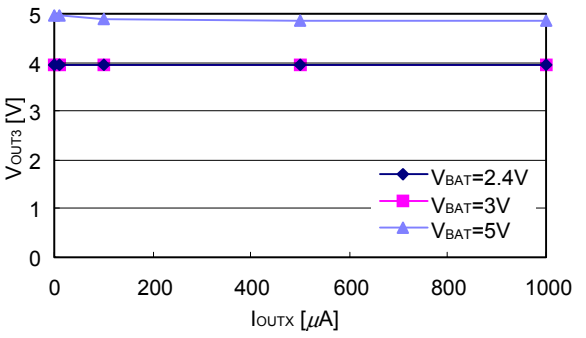
DC/DC U part output voltage (EV = Min.)



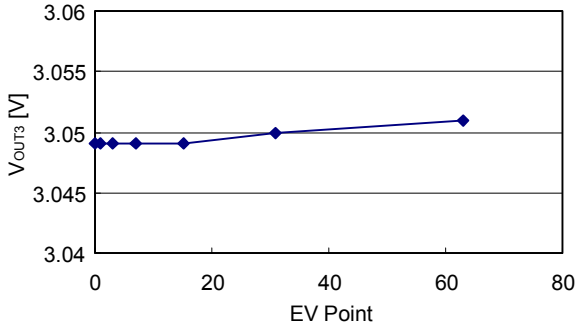
DC/DC U part output voltage (EV = Mid.)



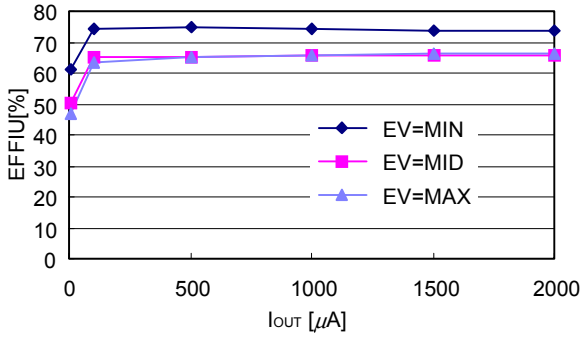
DC/DC U part output voltage (EV = Max.)



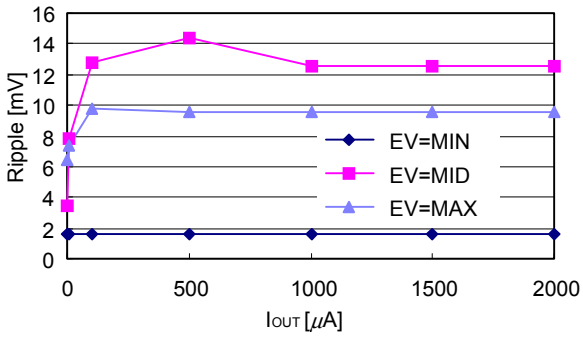
DC/DC U part output voltage (V_{BAT} = 3.0 V, V_{REFU} = 2.90 V)



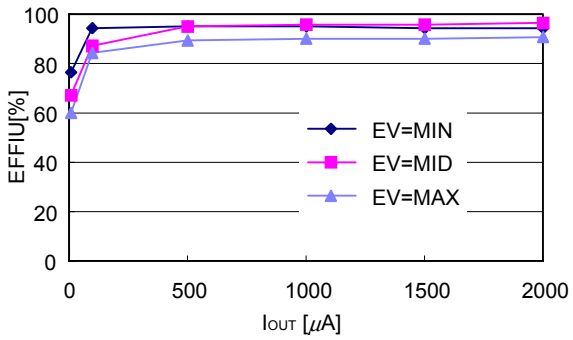
DC/DC U part output efficiency (V_{BAT} = 2.4 V)



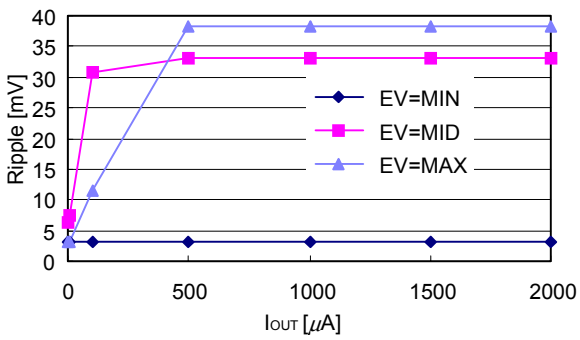
DC/DC U part output ripple voltage
(V_{BAT} = 2.4 V, reference value)



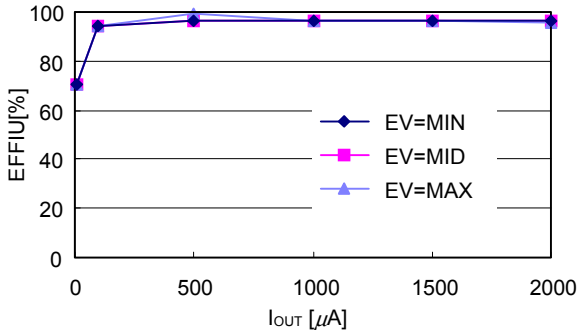
DC/DC U part output efficiency (V_{BAT} = 3.0 V)



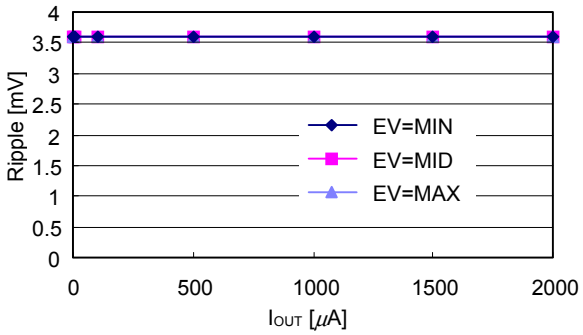
DC/DC U part output ripple voltage
(V_{BAT} = 3.0 V, reference value)



DC/DC U part output efficiency (V_{BAT} = 5.0 V)

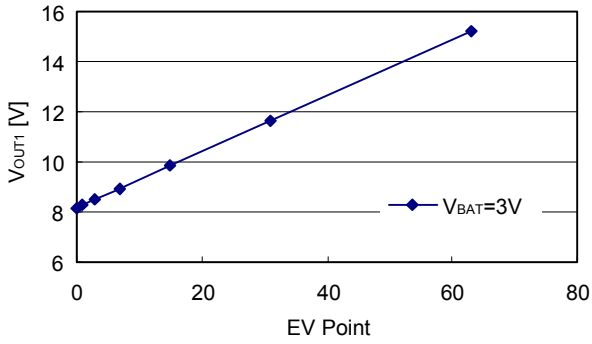


DC/DC U part output ripple voltage
(V_{BAT} = 5.0 V, reference value)

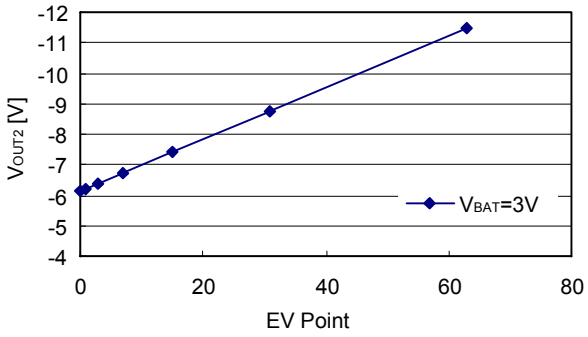


3. S-8335A200FT (1/200 duty. Unless otherwise specified, these graphs show typical data for T_{OPR} = 25°C.)

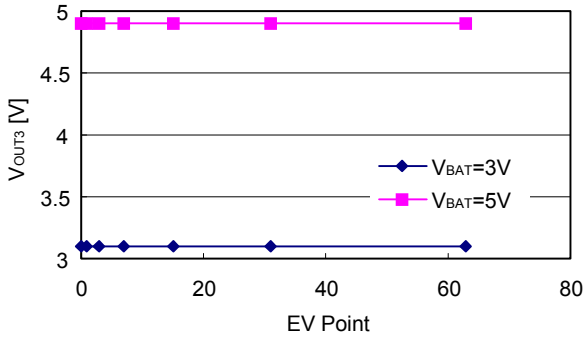
DC/DC P part output voltage



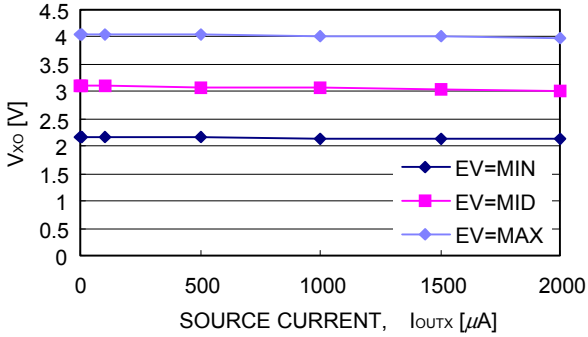
DC/DC Q part output voltage



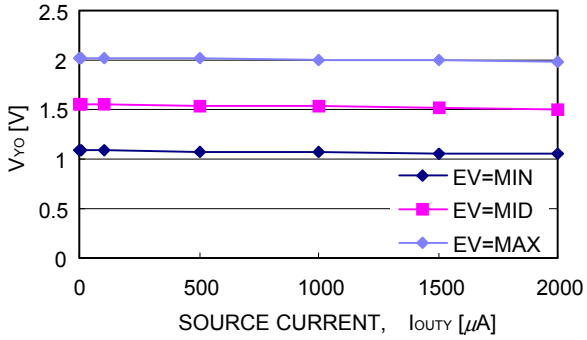
DC/DC U part output voltage (V_{REFU} = 2.91 V)



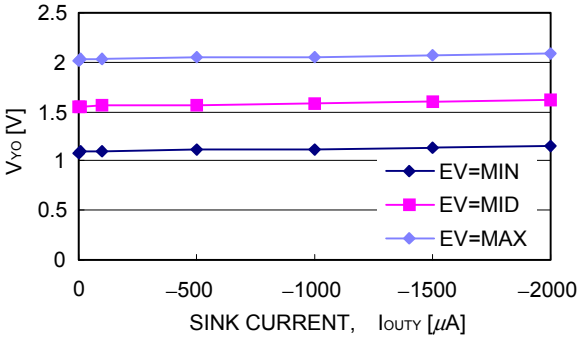
OP amplifier X part output voltage
(vs. source current, V_{BAT} = 3.0 V)



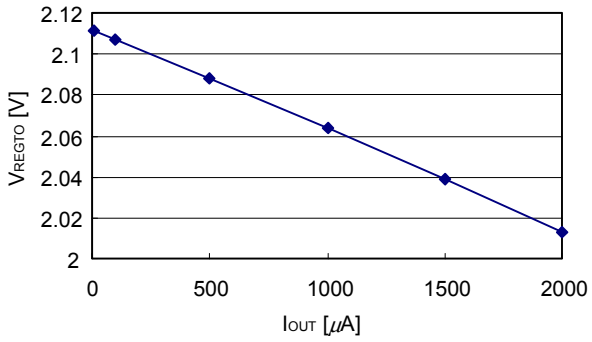
OP amplifier Y part output voltage
(vs. source current, V_{BAT} = 3.0 V)



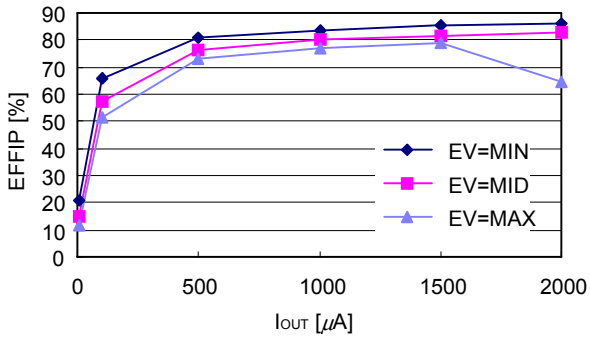
OP amplifier Y part output voltage
(vs. sink current, V_{BAT} = 3.0 V)



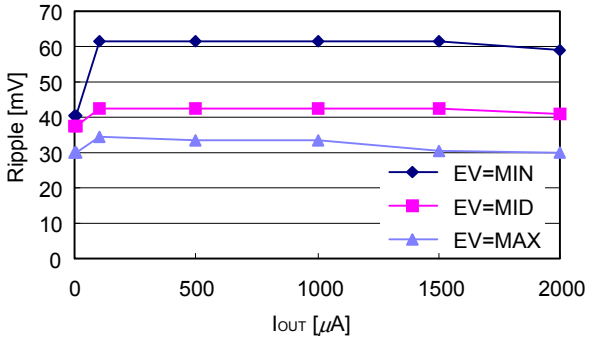
Regulator T part output voltage (V_{BAT} = 3.0 V)



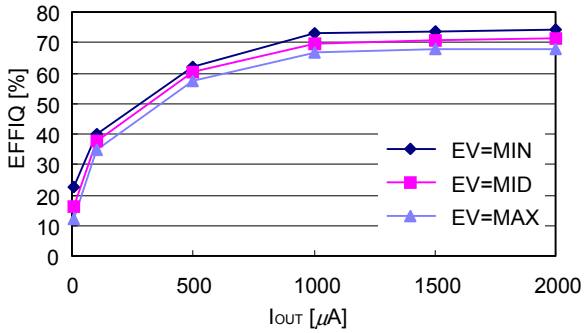
DC/DC P part output efficiency (V_{BAT} = 3.0 V)



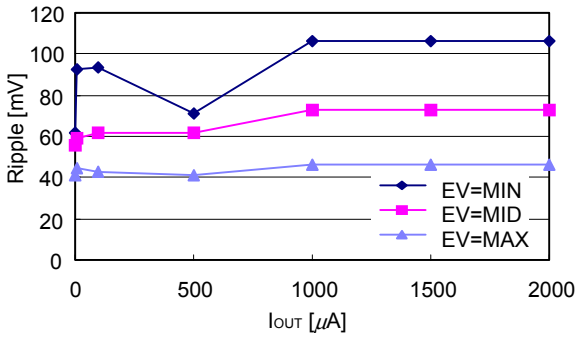
DC/DC P part output ripple voltage
(V_{BAT} = 3.0 V, reference value)



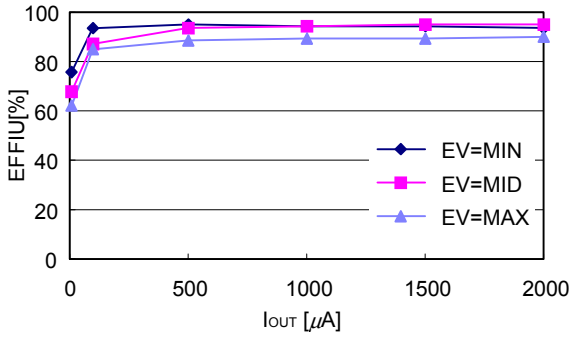
DC/DC Q part output efficiency (V_{BAT} = 3.0 V)



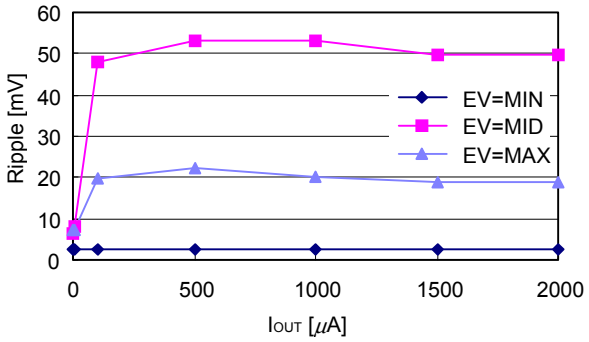
DC/DC Q part output ripple voltage
(V_{BAT} = 3.0 V, reference value)



DC/DC U part output efficiency (V_{BAT} = 3.0 V)

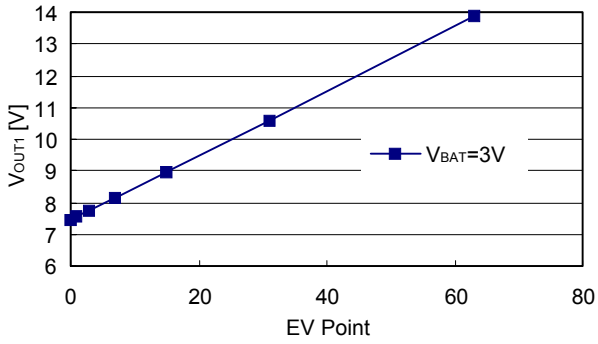


DC/DC U part output ripple voltage
(V_{BAT} = 3.0 V, reference value)

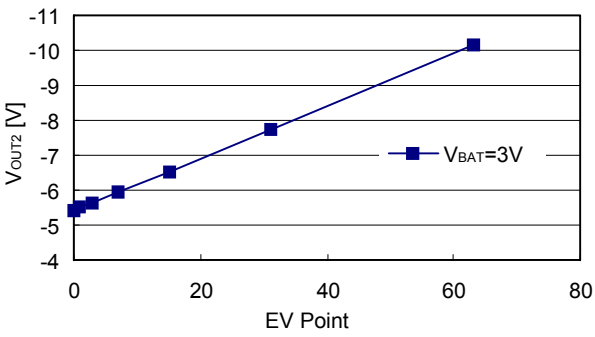


4. S-8335A160FT (1/160 duty. Unless otherwise specified, these graphs show typical data for T_{OPR} = 25°C.)

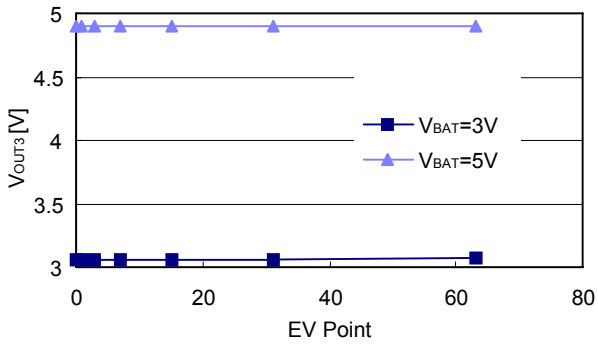
DC/DC P part output voltage



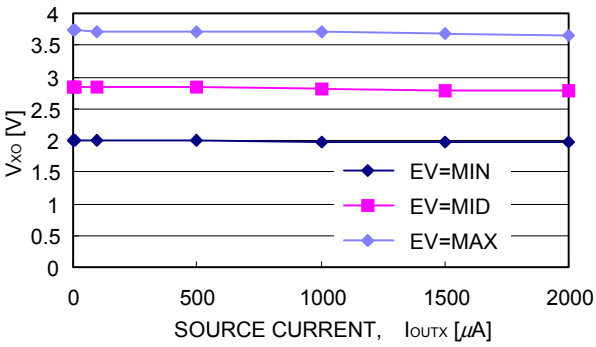
DC/DC Q part output voltage



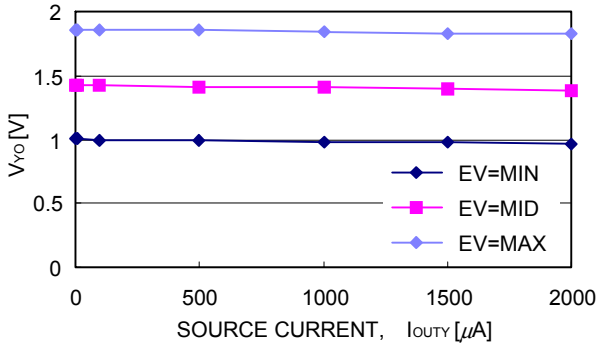
DC/DC U part output voltage (V_{REFU} = 2.906 V)



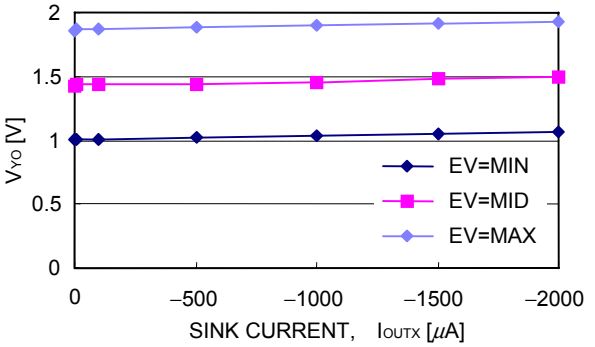
OP amplifier X part output voltage
(vs. source current, V_{BAT} = 3.0 V)



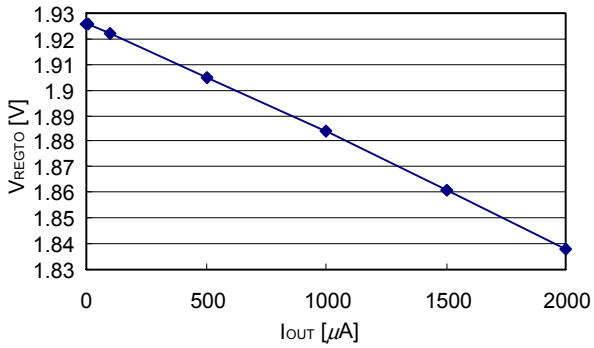
OP amplifier Y part output voltage
(vs. source current, V_{BAT} = 3.0 V)



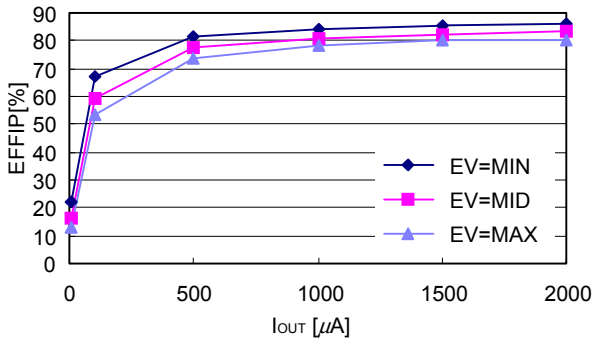
OP amplifier Y part output voltage
(vs. sink current, V_{BAT} = 3.0 V)



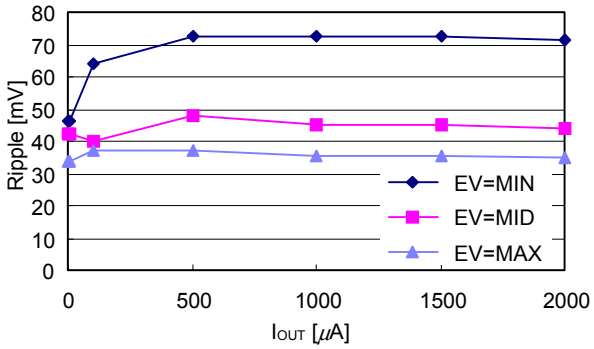
Regulator T part output voltage (V_{BAT} = 3.0 V)



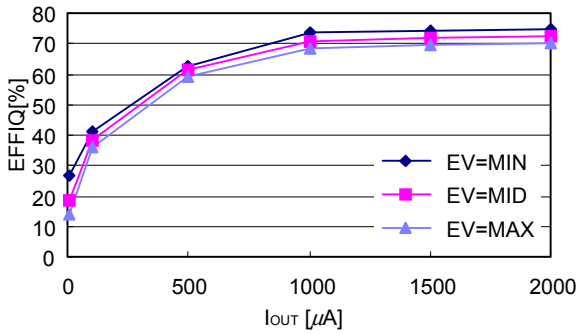
DC/DC P part output efficiency (V_{BAT} = 3.0 V)



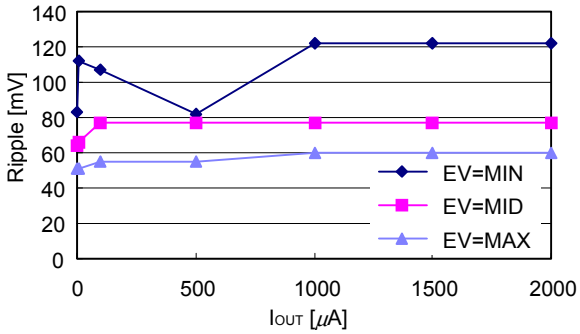
DC/DC P part output ripple voltage (V_{BAT} = 3.0 V, reference value)



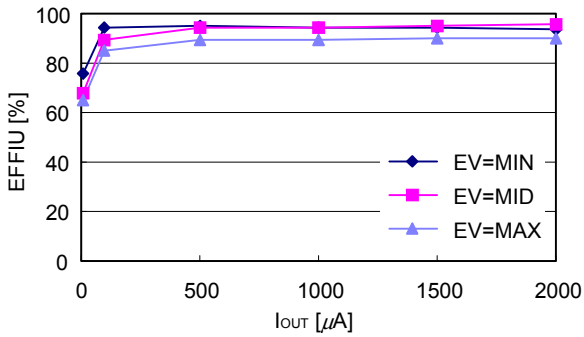
DC/DC Q part output efficiency (V_{BAT} = 3.0 V)



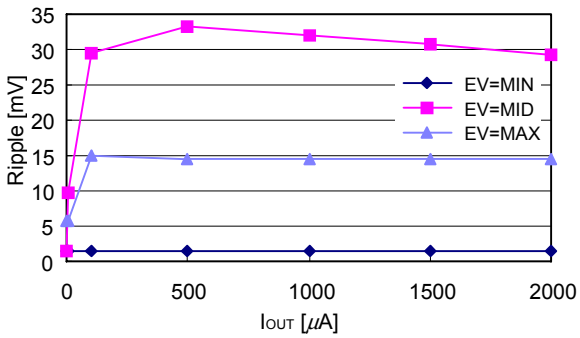
DC/DC Q part output ripple voltage (V_{BAT} = 3.0 V, reference value)



DC/DC U part output efficiency (V_{BAT} = 3.0 V)

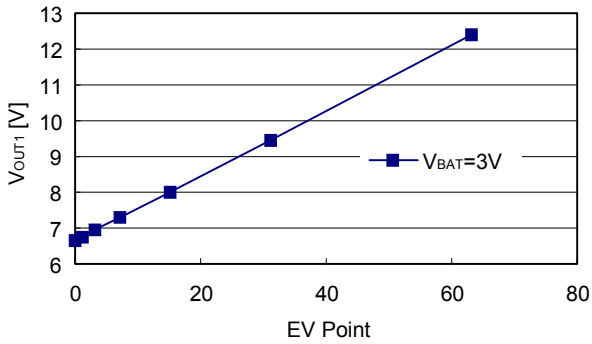


DC/DC U part output ripple voltage (V_{BAT} = 3.0 V, reference value)

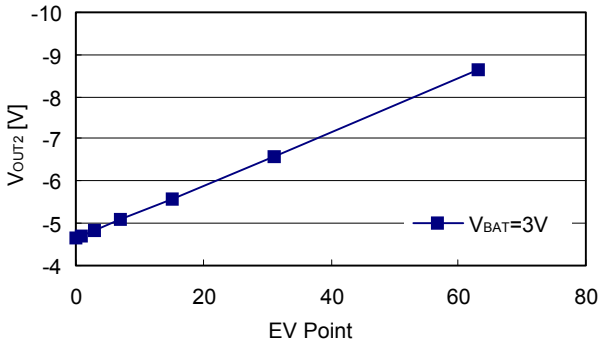


5. S-8335A120FT (1/120 duty. Unless otherwise specified, these graphs show typical data for T_{OPR} = 25°C.)

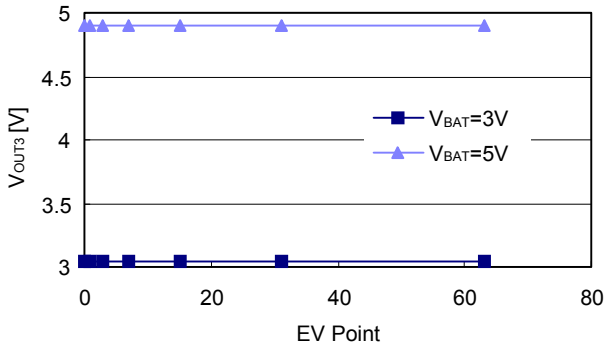
DC/DC P part output voltage



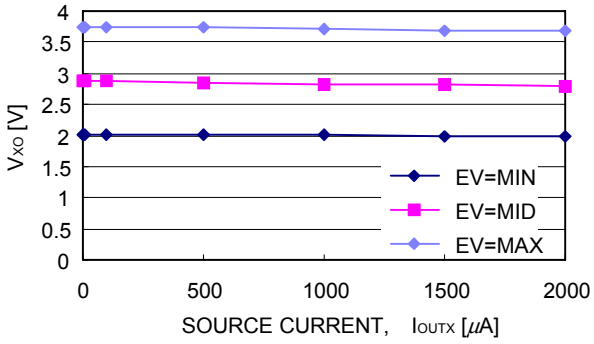
DC/DC Q part output voltage



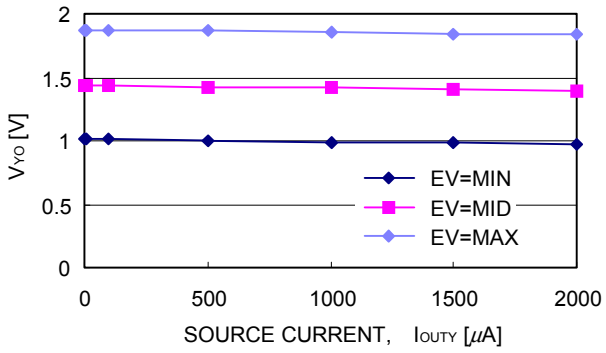
DC/DC U part output voltage (V_{REFU} = 2.92 V)



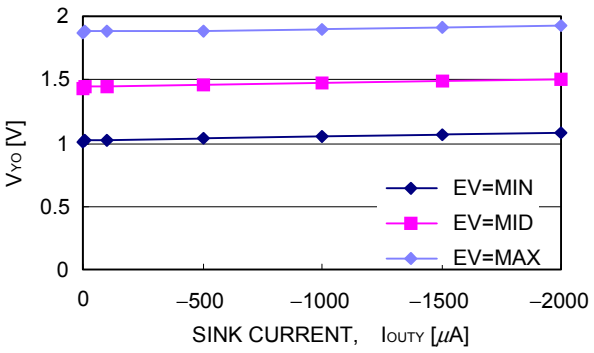
OP amplifier X part output voltage
(vs. source current, V_{BAT} = 3.0 V)



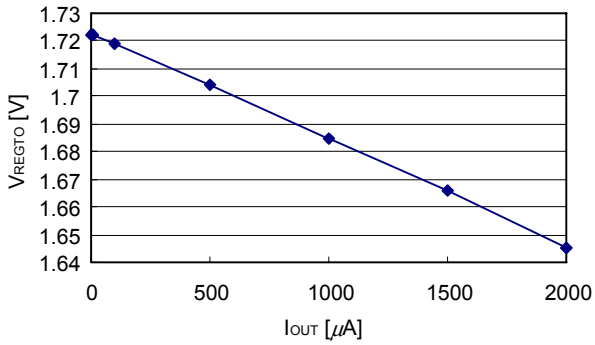
OP amplifier Y part output voltage
(vs. source current, V_{BAT} = 3.0 V)



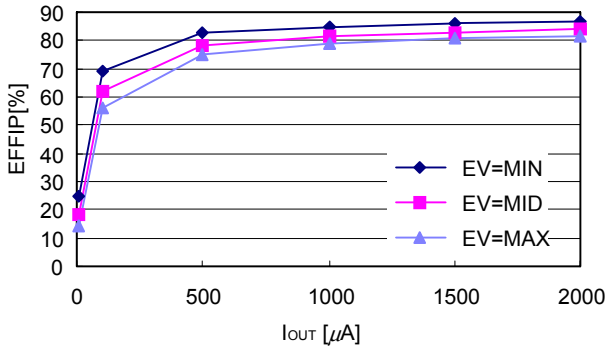
OP amplifier Y part output voltage
(vs. sink current, V_{BAT} = 3.0 V)



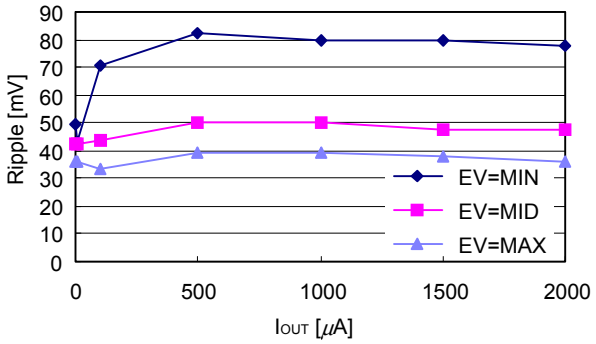
Regulator T part output voltage (V_{BAT} = 3.0 V)



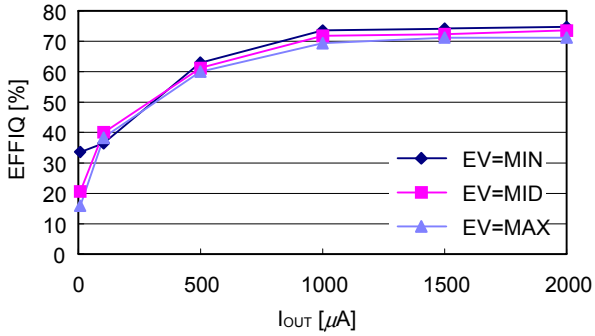
DC/DC P part output efficiency (V_{BAT} = 3.0 V)



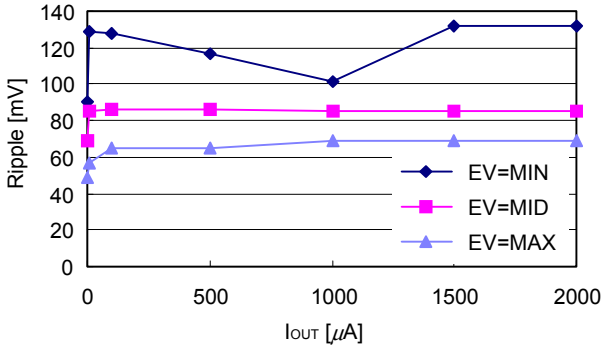
DC/DC P part output ripple voltage
(V_{BAT} = 3.0 V, reference value)



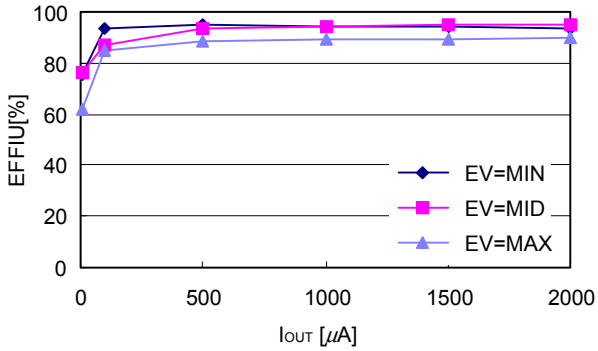
DC/DC Q part output efficiency (V_{BAT} = 3.0 V)



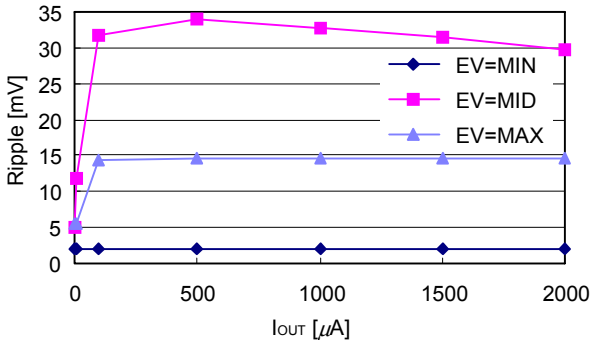
DC/DC Q part output ripple voltage
(V_{BAT} = 3.0 V, reference value)

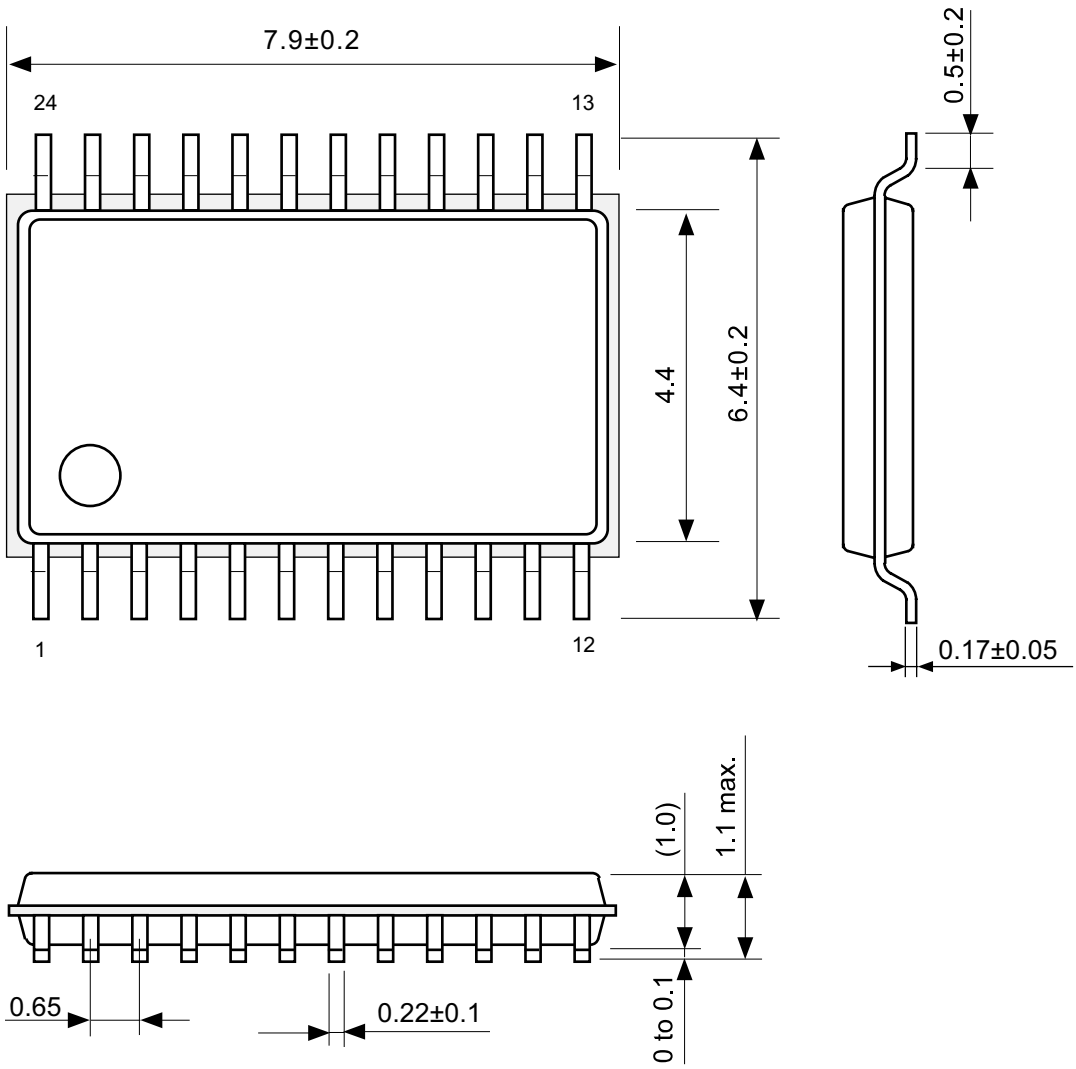


DC/DC U part output efficiency (V_{BAT} = 3.0 V)



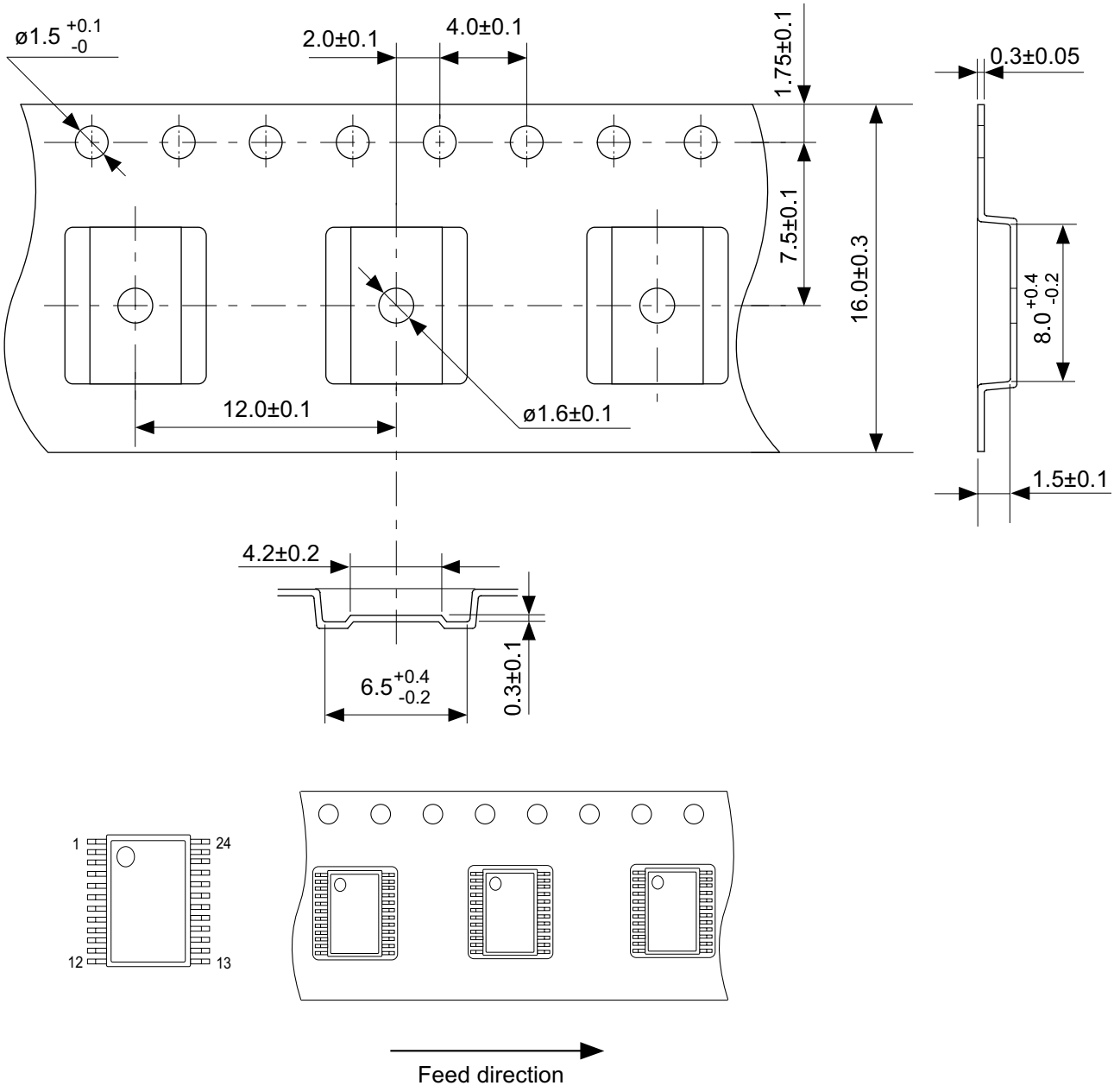
DC/DC U part output ripple voltage
(V_{BAT} = 3.0 V, reference value)





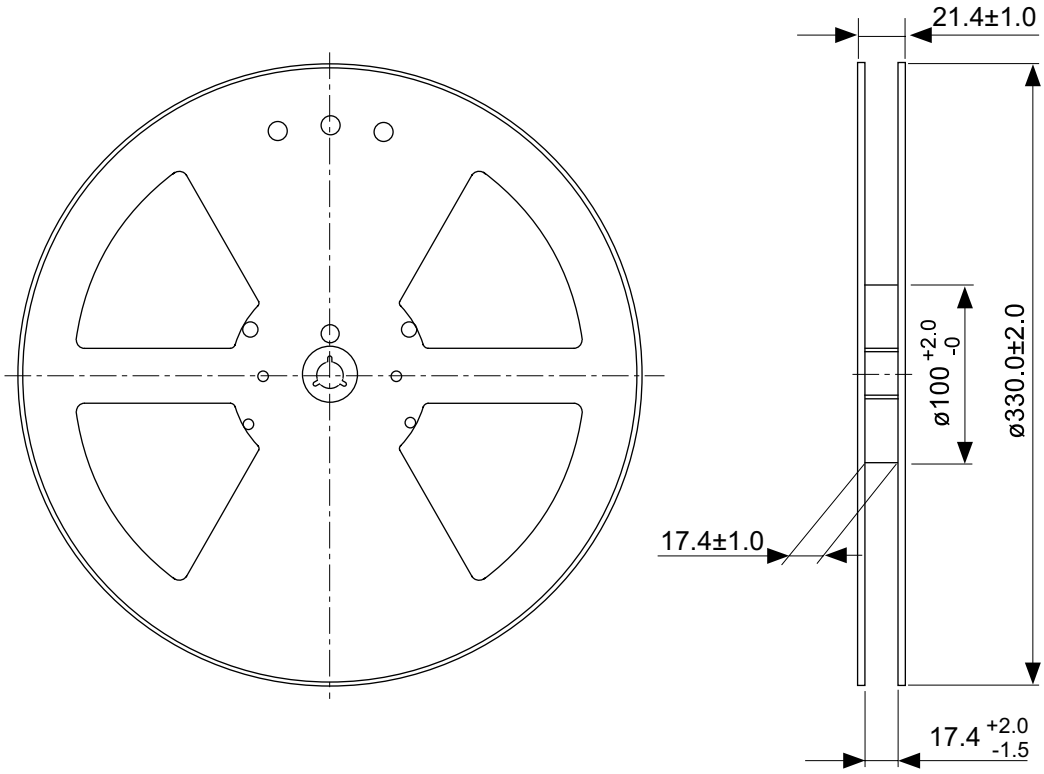
No. FT024-A-P-SD-1.0

TITLE	TSSOP24-A-PKG Dimensions
No.	FT024-A-P-SD-1.0
SCALE	
UNIT	mm
Seiko Instruments Inc.	

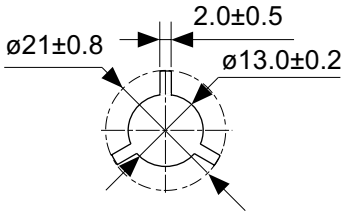


No. FT024-A-C-SD-1.0

TITLE	TSSOP24-A-Carrier Tape
No.	FT024-A-C-SD-1.0
SCALE	
UNIT	mm
Seiko Instruments Inc.	



Enlarged drawing in the central part



No. FT024-A-R-SD-1.0

TITLE	TSSOP24-A-Reel		
No.	FT024-A-R-SD-1.0		
SCALE		QTY.	2,000
UNIT	mm		
Seiko Instruments Inc.			

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