PIC18F1220/1320

PIC18F1220/1320 Rev. B1 Silicon/Data Sheet Errata

The PIC18F1220/1320 Rev. B1 parts you have received conform functionally to the Device Data Sheet (DS39605**C**), except for the anomalies described below.

All of the issues listed here will be addressed in future revisions of the PIC18F1220/1320 silicon.

The following silicon errata apply only to PIC18F1220/1320 devices with these Device/Revision IDs:

Part Number	Device ID	Revision ID
PIC18F1220	00 0111 111	00010
PIC18F1320	00 0111 110	00010

The Device IDs (DEVID1 and DEVID2) are located at addresses 3FFFFEh:3FFFFFh in the device's configuration space. They are shown in hexadecimal in the format "DEVID2 DEVID1".

1. Module: Core

Certain combinations of code sequence, code placement, VDD, FOSC and temperature may cause the corruption of fetched instructions. A corrupted instruction fetch will cause the part to execute an incorrect instruction with unpredictable results.

Microchip cannot predict which combinations of these conditions will cause this failure.

If this failure mechanism exists in your system, it should become evident during statistically significant preproduction testing using your particular code sequence and placement (the minimum suggested sample size is 100 units). Preproduction testing should exercise all the functions of your application across system variables. Any changes to code should be tested in the same manner prior to being implemented.

This issue has not been observed for FOSC up to 4 MHz with VDD up to 5.25V. If failures occur while meeting both of these conditions, then the failures are likely not related to this failure mechanism.

Work around

Use the part at or below 4 MHz with VDD at or below 5.25V.

Change the placement of code within program memory.

Use the next revision of silicon when it becomes available.

Date Codes that pertain to this issue:

All engineering and production devices.

2. Module: Data EEPROM

When reading the data EEPROM, the contents of the EEDATA register may be corrupted if the RD bit (EECON1<0>) is set immediately following a write to the address byte (EEADR). The actual contents of the data EEPROM remain unaffected.

Work around

Do not set EEADR immediately before the execution of a read. Write to EEADR at least one instruction cycle before setting the RD bit. The instruction between the write to EEADR and the read can be any valid instruction, including a NOP.

Date Codes that pertain to this issue:

All engineering and production devices.

3. Module: Core (DAW Instruction)

The DAW instruction may improperly clear the Carry bit (STATUS<0>) when executed.

Work around

Test the Carry bit state before executing the DAW instruction. If the Carry bit is set, increment the next higher byte to be added, using an instruction such as INCFSZ (this instruction does not affect any Status flags and will not overflow a BCD nibble). After the DAW instruction has been executed, process the Carry bit normally (see Example 1).

EXAMPLE 1: PROCESSING THE CARRY BIT DURING BCD ADDITIONS

```
MOVLW   0x80        ; .80 (BCD)
ADDLW   0x80        ; .80 (BCD)

BTFSC   STATUS, C   ; test C
INCFSZ  byte2       ; inc next higher LSB
DAW
BTFSC   STATUS, C   ; test C
INCFSZ  byte2       ; inc next higher LSB

This is repeated for each DAW instruction.
```

Date Codes that pertain to this issue:

All engineering and production devices.

4. Module: INTOSC

Incrementing or decrementing the value in the OSCTUNE register may not have the expected effect of shifting the INTRC or INTOSC output frequencies. The OSCTUNE values for which this happens may vary with temperatures above 70°C.

Work around

None

Date Codes that pertain to this issue:

All engineering and production devices.

5. Module: Internal Oscillator Block

At high temperature (above 85°C) or low VDD (below 2.5V), the IOFS bit (OSCCON<2>) may not become set when the internal oscillator block is selected as the system clock source for any frequency above 31 kHz (OSCCON<6:4> ≠ 000). The INTOSC output will stabilize at 8 MHz; however, the IOFS bit may not become set.

Work around

If time critical code is to be executed, it should be delayed by 1 ms following the operation that enables the 8 MHz INTOSC output from the internal oscillator block.

Date Codes that pertain to this issue:

All engineering and production devices.

6. Module: Internal Oscillator Block

If the INTRC clock source was not started at POR (any VDD) and VDD is greater than 4.5V, the INTRC clock source may not start or may require a long delay when starting. The INTRC may not restart when VDD is lowered below 4.5V.

Features that depend on the operation of the INTRC clock source may be affected. These include the INTOSC output when exiting from Sleep mode, the Watchdog Timer (WDT) if enabled by firmware using the WDTCON register, Two-Speed Start-ups during Reset or wake-up from Sleep and the Fail-Safe Clock Monitor (FSCM) when exiting Sleep mode.

The INTOSC frequency may rise very high (for example, 9.5 MHz). The WDT and the FSCM may simply not function. Two-Speed Start-ups may not occur but execution will start once the primary clock source becomes ready.

Work around

Several work arounds may be used.

1. Enable the WDT in Configuration register, CONFIG2H, and place a `CLRWDT` instruction somewhere in the main loop.
2. Configure the internal oscillator block as the primary clock source using Configuration Register 1H.
3. Any technique that starts the INTRC at Reset and does not disable it may be used.
4. Ensure that VDD is below 4.5V when starting the INTRC clock source.

There may be other work arounds.

Date Codes that pertain to this issue:

All engineering and production devices.

7. Module: EUSART

The CREN bit may be cleared when the EUSART completes an auto-baud measurement.

Work around

When the auto-baud measurement is complete, the CREN bit must be set by firmware.

Date Codes that pertain to this issue:

All engineering and production devices.

8. Module: EUSART

If the TXEN bit is set when an auto-baud measurement is completed, the EUSART may transmit an arbitrary byte.

Work around

Clear the TXEN bit before performing the auto-baud measurement. When the measurement is complete, set the TXEN bit.

Date Codes that pertain to this issue:

All engineering and production devices.

9. Module: EUSART

The auto-baud measurement may not determine the correct baud rate if the ABDEN bit is set while the RB4/RX pin is low.

Work around

If the wake-up function is being used (WUE is set), wait for the RB4/RX pin to go high following a Break signal before setting the ABDEN bit.

If the wake-up function is not being used, ensure that RB4/RX is Idle (high between bytes) before setting the ABDEN bit.

Date Codes that pertain to this issue:

All engineering and production devices.

10. Module: Data EEPROM

When writing to the data EEPROM, the contents of the data EEPROM memory may not be written as expected.

Work around

Either of two work arounds can be used:

1. Before beginning any writes to the data EEPROM, enable the LVD (any voltage) and wait for the internal voltage reference to become stable. LVD interrupt requests may be ignored. Once the LVD voltage reference is stable, perform all EEPROM writes normally. When writes have been completed, the LVD may be disabled.
2. Configure the BOR as enabled (any voltage). Select a threshold below V_{DD} to allow normal operation. If V_{DD} is below the BOR threshold, the device will be held in Brown-out Reset.

Date Codes that pertain to this issue:

All engineering and production devices.

11. Module: Reset

It has been observed that in certain Reset conditions, including power-up, the first `GOTO` instruction at address 0x0000 may not be executed. This occurrence is rare and affects very few applications.

To determine if your system is affected, test a statistically significant number of applications across the operating temperature, voltage and frequency ranges of the application. Affected systems will repeatably fail normal testing. Systems not affected will continue to not be affected over time.

Work around

Insert a `NOP` instruction at address 0x0000.

Date Codes that pertain to this issue:

All engineering and production devices.

Clarifications/Corrections to the Data Sheet

In the Device Data Sheet (DS39605**C**), the following clarifications and corrections should be noted.

1. Module: CCP

In **Section 14.0 "Timer3 Module"**, bit 6 of the T3CON register was incorrectly defined as "unimplemented". The correct definition for T3CON<6> is T3CCP2 and is shown in **bold** below:

REGISTER 14-1: T3CON: TIMER3 CONTROL REGISTER

R/W-0	**R/W-0**	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RD16	**T3CCP2**	T3CKPS1	T3CKPS0	T3CCP1	$\overline{\text{T3SYNC}}$	TMR3CS	TMR3ON
bit 7							bit 0

bit **6**, 3 **T3CCP2:T3CCP1:** Timer3 and Timer1 to CCP Enable bits
1x = Timer3 is the clock source for compare/capture CCP module
01 = Reserved
00 = Timer1 is the clock source for compare/capture CCP module

2. Module: Data EEPROM Memory

In Table 22-1 on page 254 of the Device Data Sheet, the typical value for parameter D122, Data EEPROM Erase/Write Cycle Time (T_{DEW}) has changed. The new value is 5.5 ms and is shown in **bold** below.

TABLE 22-1: MEMORY PROGRAMMING REQUIREMENTS

DC CHARACTERISTICS			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D122	T_{DEW}	Erase/Write Cycle Time	—	**5.5**	—	ms	

REVISION HISTORY

Rev A Document (06/2003)

First revision of this document, silicon issues 1 (Data EEPROM), 2 (Data EEPROM), 3 (Core), 4 (INTOSC), 5 (Internal Oscillator Block), 6 (Internal Oscillator Block), 7 (Electrical Specifications), 8 (EAUSART), 9 (EAUSART) and 10 (EAUSART) and Data Sheet Clarification issues 1 (Internal RC Accuracy) and 2 (DC Characteristics Table).

Rev B Document (10/2003)

Added silicon issue 1 (Core).

Rev C Document (12/2003)

Removed silicon issue 2 (Data EEPROM). Changed silicon issue 8, 9 and 10 (was issue 9, 10 and 11) from EAUSART to USART. Added silicon issue 11 (Data EEPROM).

Rev D Document (05/2005)

Removed silicon issue 7 (Electrical Specifications), added silicon issue 11 (Reset), changed previous label of USART to EUSART in silicon issues 7, 8 and 9 (to be consistent with the data sheet) and added Data Sheet Clarification issue 1 (CCP).

Rev E Document (08/2005)

Added Data Sheet Clarification issue 2 (Data EEPROM Memory).

Rev F Document (03/2006)

Corrected part number revision IDs in the table on page one.

NOTES:

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02/16/06