# SiT6096EBB Evaluation Board User Manual for SiT153x/4x Ultra-Low power 32kHz Oscillators



## 1 SiT6096EBB Evaluation Boards Introduction

The SiT6096EBB evaluation board provides the ability to evaluate the functionality of SiT153x/4x 32kHz oscillators on a simple board that makes it easy to power up the oscillator and observe the output buffered through an operational amplifier. The analog buffer isolates the device from the significant loading, which is important for performing best waveform and current measurements.

The SiT6096EBB supports the following package sizes: 2.0 x 1.2 mm.

## 2 Board information

A PCB view of the SiT6096EBB board with component reference designator call out is shown in Figure A2 (SiT6096EBB layout).

# 3 Connectors

**Overview:**

| Designator | Purpose |
|---|---|
| J2 | DUT Power |
| J3 | Buffer Power |
| J1 | Buffer output |
| J6 | Direct output |
| J4 | DUT Consumption Current measurement |

**Mating connectors:**

| Designator | Mating connectors (Digi-Key Part Numbers) |
|---|---|
| J2 | WM2613-ND |
| J3 | WM2626-ND |
| J4 | WM2613-ND |
| Crimps for J2, J3, J4 | WM6685CT-ND, 7pcs |
| J6 | H2011-ND |
| Crimps for J6 | H9999-ND, 2pcs |
| J1 | A97594-ND |

Pin-1 orientation of the chip is defined by a chamfer and dot in the silkscreen pattern.

## *3.1 DUT Power*

Evaluation boards have input two-pin connector J2 for power supply. Pins polarities are identified on the silkscreen pattern near connector.

## *3.2 Buffered Clock Output*

This EVB uses an operational amplifier to buffer the oscillator clock output to make it easy to connect to test and measurement equipment through SMA cables without loading the ultra-low power clock output driver. The ADA4817-1 FET operational amplifier is used in a unity gain buffer configuration. It is a unity-gain stable, ultra-high speed, voltage feedback amplifier with FET inputs.

The three-pin connector J3 is intended for supplying the VDD power to the on-board operational amplifier. Pin polarities are identified on the silkscreen pattern near connector J3. The operational amplifier requires a dual power supply and should be -3V for negative power rail (V-) and +8V for the positive supply (V+).

**Buffer supply voltage:**

| Power rail name | Voltage |
|---|---|
| V+ | +8V (max) |
| V- | -3V (min) |

## *3.3 Clock Output (Direct)*

The oscillator output is best observed through the buffered output path, using a test probe placed on the test point TP2 or through the SMA connector J1. The buffer can be bypassed and the output can be directly observed thru J6 2mm pitch pin header connector or using test point TP1 (see Figures A2-A3 of Appendix A for test points arrangement on the board). Section 4.1 shows recommended measurement configurations. When probing the oscillator output directly, the probe loading can affect the output waveform and power consumption of the device. SiTime recommends active probes with 10MΩ and 1pF impedance.

### 3.4 DUT Current Consumption Measurement

Two-pin connector J4 enables measuring the current consumption of the SiT153x/4x device. To measure the current properly, remove zero-ohm resistor R3, and connect the DMM or other current measuring device across this connector.

# 4 Application Notes

### 4.1 Configurations

SiT6096EBB supports multiple configurations for evaluating AC and DC coupled output modes of SiTime SiT153x/4x oscillator. In addition, this EVB provides the ability to add additional load capacitance and to bypass the output buffer. Figure A1 (see Appendix A) shows the schematic of SiT6096EBB. Components labeled “DNP” are not assembled. Components which are common to all listed bellow configurations have nominal values assigned to them.

### 4.2 General Configuration

Figure 1 shows general shipment configuration.

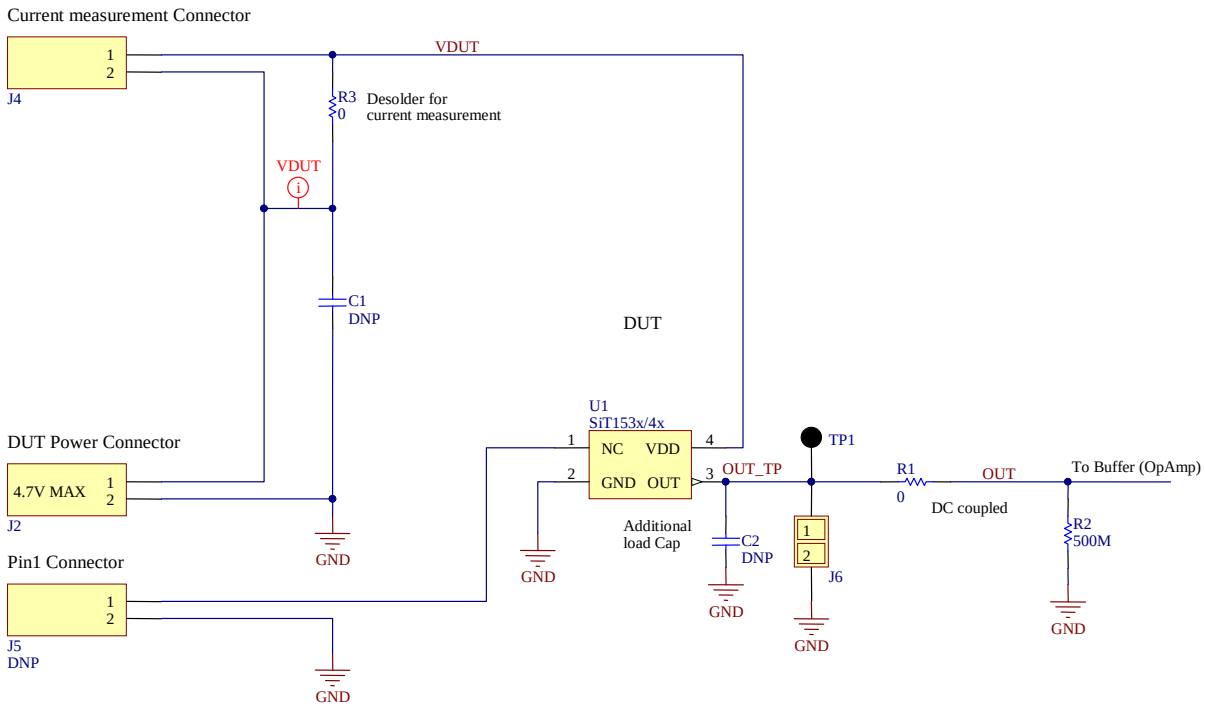


Figure 1: General EVB Configuration

### 4.2.1 Configuration 1: DC-Coupled Output

This configuration is intended for observing a DC coupled output through an oscilloscope through the buffered output at SMA (J1) connector or test point (TP2) (see Figures A1-A2 of Appendix A for test point locations on the board). Figure 2 shows the circuit for this configuration.

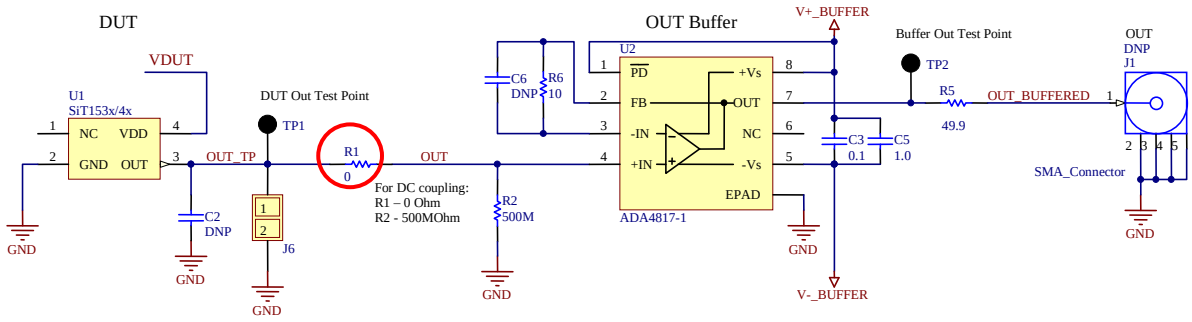


Figure 2: DC-Coupled Output Configuration

### 4.2.2 Configuration 2: AC-Coupled Output

This configuration is intended for observing an AC-coupled output through an oscilloscope through the buffered output at SMA (J1) connector or Buffer output test point (TP2) (see Figures A1-A2 of Appendix A for test point locations on the board). A 0.1µF capacitor is placed in the clock output signal path. Figure 3 shows the circuit for this configuration.

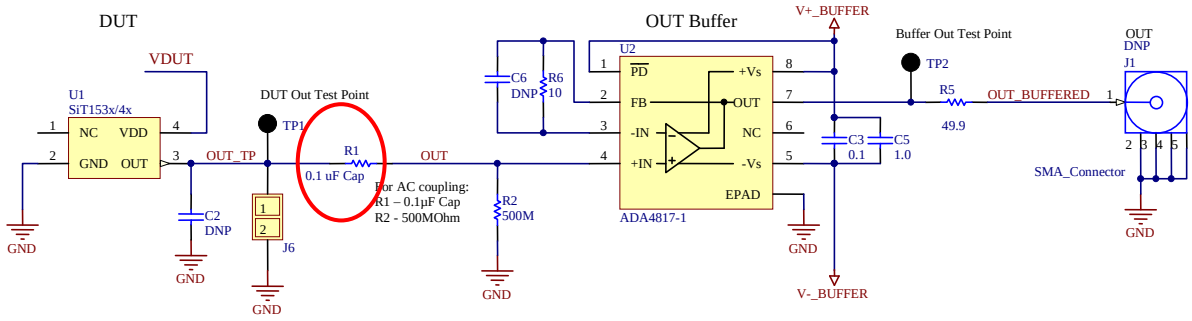


Figure 3: AC-Coupled Output Configuration

### 4.2.3 Configuration 4: Direct Output with Additional Load Capacitor

This configuration is intended for observing direct oscillator output with a passive high input impedance (> 1 MΩ || < 1 pf) scope probe at test point TP1 (see Figures A1-A2 of Appendix A for test points on the board) or to connect the oscillator output to end user system using 2 mm pitch header connector J6 with an optional user defined load capacitor C2. Figure 4 shows the circuit for this configuration.

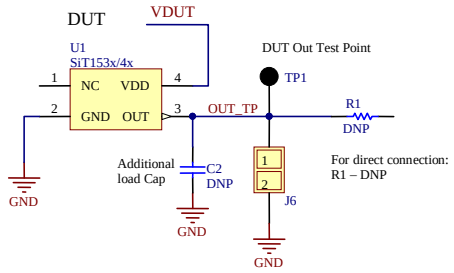


Figure 4: Circuit for observing direct oscillator output.

### 4.2.4 Configuration 5: DUT Power Supply Filter

This configuration intended for providing power filter for oscillator by soldering user defined capacitor C1. Figure 5 shows circuit for this configuration. The DUT power filtering is not required in common cases. It should be used only if power supply noise is significant or to cancel parasitic inductance effect of long wires from Power Supply to EVB.

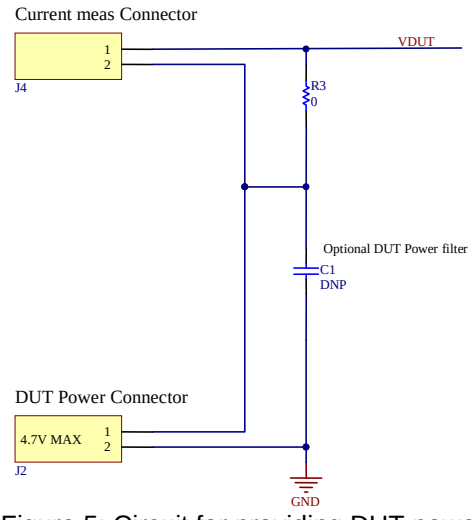


Figure 5: Circuit for providing DUT power filter.

### 4.2.5 Measuring SiT153x/4x Current Consumption

When measuring the SiT153x/4x supply current, simply remove jumper resistor R3 using 2-pin connector J4. Figure 6 shows circuit for this configuration and connect a precision DMM to connector J4.
**DUT current consumption: approximately 800 nA (no load), $T_A$ = 25°C**

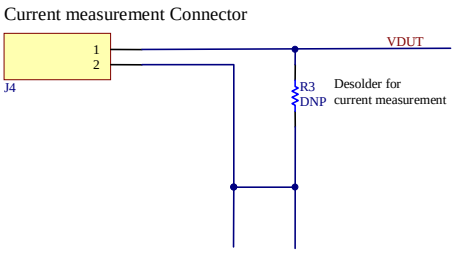


Figure 6: DUT Supply Current Measurement.

# Appendix A

## A1: Board schematic

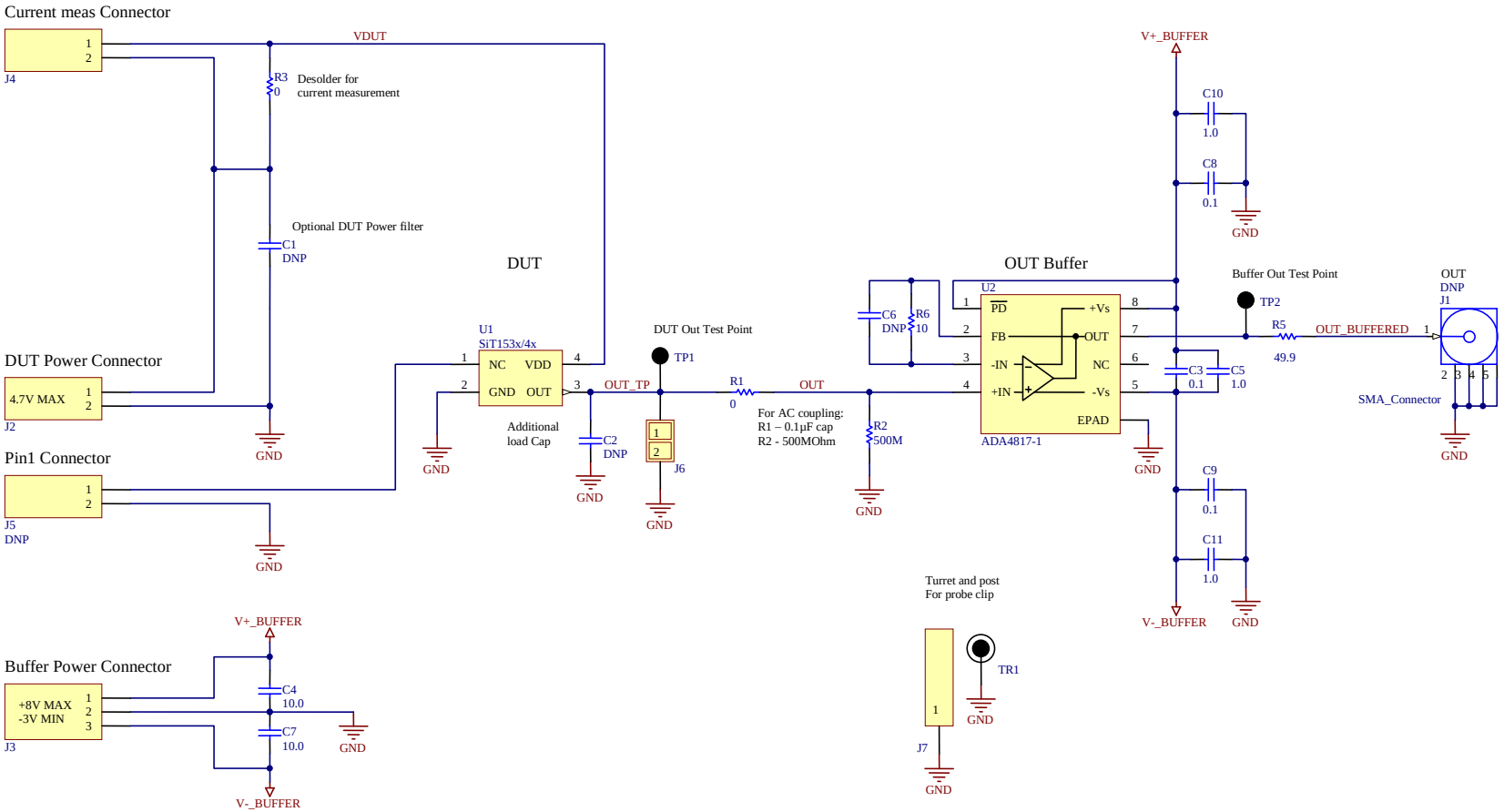


**Figure A1: SiT6096EBB schematic**

# A2: Board layout

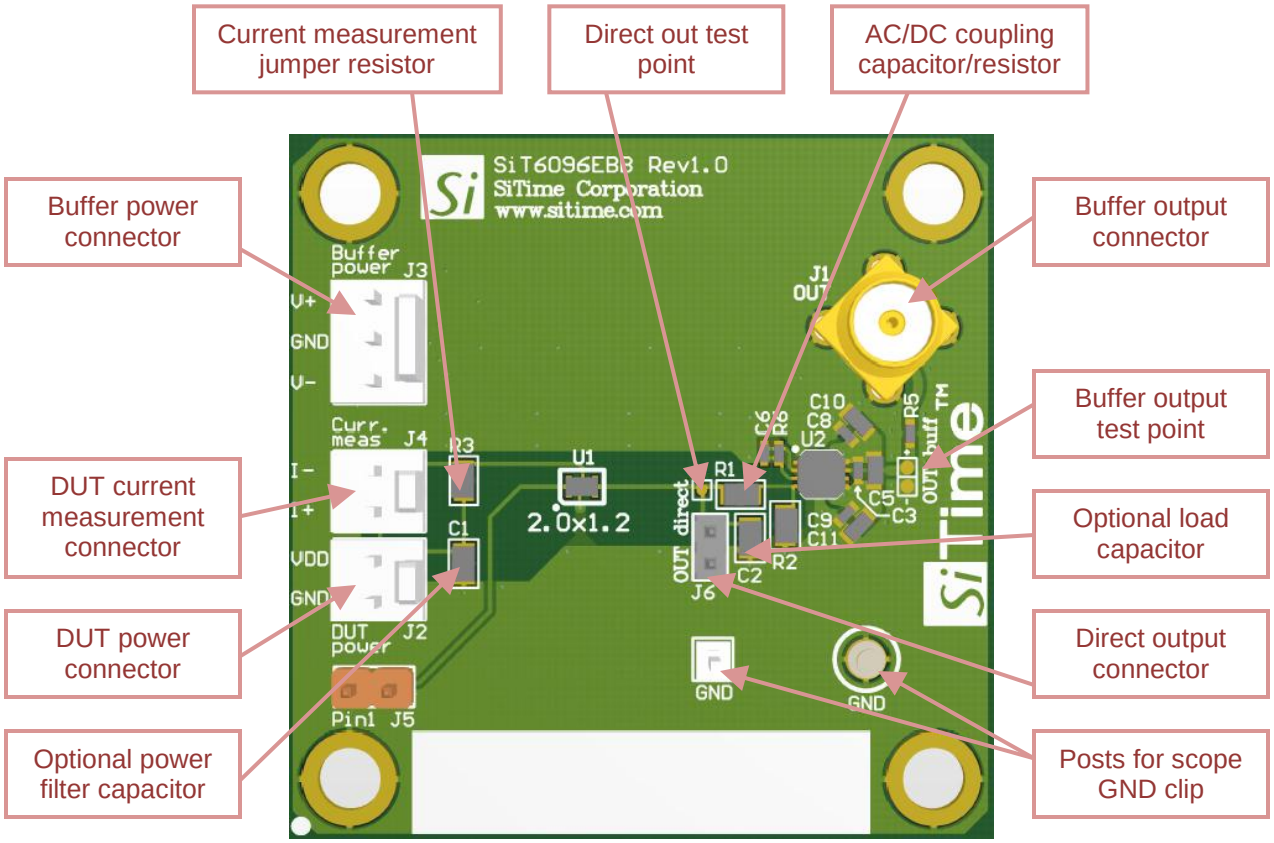


**Figure A2: SiT6096EBB layout**

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