Low Power Video Difference Amplifier

FEATURES

- Differential or Single-Ended Gain Block (Adjustable)
- –3dB Bandwidth, $A_V = \pm 10$ 35MHz
- Slew Rate 220V/μs
- Low Supply Current 13mA
- Output Current ±20mA
- CMRR at 10MHz 48dB
- LT1193 Pin Out
- Low Cost
- Single 5V Operation
- Drives Cables Directly
- Output Shutdown

APPLICATIONS

- Line Receivers
- Video Signal Processing
- Cable Drivers
- Tape and Disc Drive Systems

DESCRIPTION

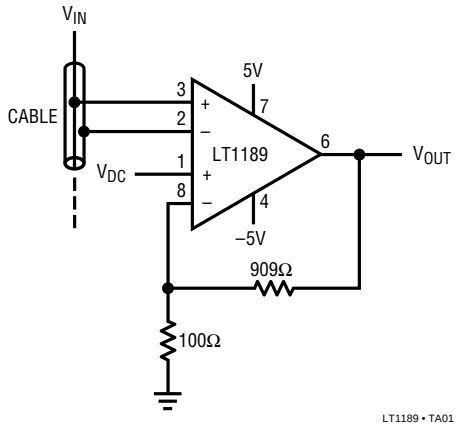
The LT1189 is a difference amplifier optimized for operation on ±5V, or a single 5V supply, and gain ≥10. This versatile amplifier features uncommitted high input impedance (+) and (–) inputs, and can be used in differential or single-ended configurations. Additionally, a second set of inputs give gain adjustment and DC control to the difference amplifier.

The LT1189's high slew rate, 220V/μs, wide bandwidth, 35MHz, and ±20mA output current require only 13mA of supply current. The shutdown feature reduces the power dissipation to a mere 15mW, and allows multiple amplifiers to drive the same cable.

The LT1189 is a low power, gain of 10 stable version of the popular LT1193, and is available in 8-pin miniDIPs and SO packages. For lower gain applications see the LT1187 data sheet.

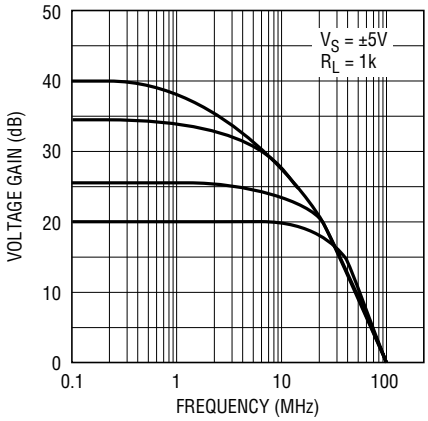
TYPICAL APPLICATION

Cable Sense Amplifier for Loop Through Connections with DC Adjust



LT1189 • TA01

Closed-Loop Gain vs Frequency



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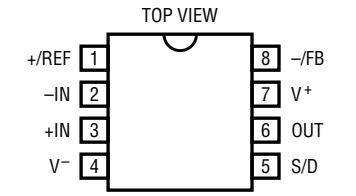
ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 18V
Differential Input Voltage ..... ±6V
Input Voltage ..... $\pm V_S$
Output Short Circuit Duration (Note 1) ..... Continuous
Operating Temperature Range
LT1189M ..... –55°C to 150°C
LT1189C ..... 0°C to 70°C
Junction Temperature (Note 2)
Plastic Package (CN8,CS8) ..... 150°C
Ceramic Package (CJ8,MJ8) ..... 175°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION



J8 PACKAGE
8-LEAD HERMETIC DIP

N8 PACKAGE
8-LEAD PLASTIC DIP

S8 PACKAGE
8-LEAD PLASTIC SOIC

LT1189 • POI01

T_{JMAX} = 175°C, θ_{JA} = 100°C/W (J8)
T_{JMAX} = 150°C, θ_{JA} = 100°C/W (N8)
T_{JMAX} = 150°C, θ_{JA} = 150°C/W (S8)

ORDER PART NUMBER
LT1189MJ8 LT1189CJ8 LT1189CN8 LT1189CS8
S8 PART MARKING
1189

±5V ELECTRICAL CHARACTERISTICS

T_A = 25°C, (Note 3)

V_S = ±5V, V_{REF} = 0V, R_{FB1} = 900Ω from pins 6 to 8, R_{FB2} = 100Ω from pin 8 to ground, R_L = R_{FB1} + R_{FB2} = 1k, C_L ≤ 10pF, pin 5 open.

SYMBOL	PARAMETER	CONDITIONS	LT1189M/C MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	Either Input, (Note 4)		1.0	3.0	mV
		SOIC Package		1.0	4.0	mV
I_{OS}	Input Offset Current	Either Input		0.2	1.0	µA
I_B	Input Bias Current	Either Input		±0.5	±2.0	µA
e_n	Input Noise Voltage	f_O = 10kHz		30		nV/√Hz
i_n	Input Noise Current	f_O = 10kHz		1.25		pA/√Hz
R_{IN}	Input Resistance	Differential		30		kΩ
C_{IN}	Input Capacitance	Either Input		2.0		pF
$V_{IN\ LIM}$	Input Voltage Limit	(Note 5)		±170		mV
	Input Voltage Range		–2.5		3.5	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = –2.5V to 3.5V	80	105		dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.375V to ±8V	75	90		dB
V_{OUT}	Output Voltage Swing	V_S = ±5V, R_L = 1k, A_V = 50	±3.8	±4.0		V
		V_S = ±8V, R_L = 1k, A_V = 50	±6.7	±7.0		
		V_S = ±8V, R_L = 300Ω, A_V = 50, (Note 3)	±6.4	±6.8		
G_E	Gain Error	V_O = ±1.0V, A_V = 10		1.0	3.5	%
SR	Slew Rate	(Note 6, 10)	150	220		V/µs
FPBW	Full Power Bandwidth	V_O = $2V_{P-P}$, (Note 7)		35		MHz
BW	Small Signal Bandwidth	A_V = 10		35		MHz
t_r, t_f	Rise Time, Fall Time	A_V = 50, V_O = ±1.5V, 20% to 80% (Note 10)	35	50	75	ns
t_{PD}	Propagation Delay	R_L = 1k, V_O = ±125mV, 50% to 50%		12		ns
	Overshoot	V_O = ±50mV		10		%
t_s	Settling Time	3V Step, 0.1%, (Note 8)		1		µs
Diff A_V	Differential Gain	R_L = 1k, A_V = 10, (Note 9)		0.6		%
Diff Ph	Differential Phase	R_L = 1k, A_V = 10, (Note 9)		0.75		DEG_{P-P}
I_S	Supply Current			13	16	mA
	Shutdown Supply Current	Pin 5 at V^-		0.8	1.5	mA

±5V ELECTRICAL CHARACTERISTICS $T_A = 25°C$, (Note 3)

$V_S = \pm5V$, $V_{REF} = 0V$, $R_{FB1} = 900\Omega$ from pins 6 to 8, $R_{FB2} = 100\Omega$ from pin 8 to ground, $R_L = R_{FB1} + R_{FB2} = 1k$, $C_L \leq 10pF$, pin 5 open.

SYMBOL	PARAMETER	CONDITIONS	LT1189M/C MIN	TYP	MAX	UNITS
$I_{S/D}$	Shutdown Pin Current	Pin 5 at V^-		5	25	µA
t_{on}	Turn On Time	Pin 5 from V^- to Ground, $R_L = 1k$		500		ns
t_{off}	Turn Off Time	Pin 5 from Ground to V^-, $R_L = 1k$		600		ns

5V ELECTRICAL CHARACTERISTICS $T_A = 25°C$, (Note 3)

$V_S^+ = 5V$, $V_S^- = 0V$, $V_{REF} = 2.5V$, $R_{FB1} = 900\Omega$ from pins 6 to 8, $R_{FB2} = 100\Omega$ from pin 8 to V_{REF}, $R_L = R_{FB1} + R_{FB2} = 1k$, $C_L \leq 10pF$, pin 5 open.

SYMBOL	PARAMETER	CONDITIONS		LT1189M/C MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	Either Input, (Note 4) SOIC Package			1.0 1.0	3.0 5.0	mV mV
I_{OS}	Input Offset Current	Either Input			0.2	1.0	µA
I_B	Input Bias Current	Either Input			±0.5	±2.0	µA
	Input Voltage Range			2.0		3.5	V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = 2.0V$ to 3.5V		80	100		dB
V_{OUT}	Output Voltage Swing	$R_L = 300\Omega$ to Ground (Note 3)	V_{OUT} High	3.6	4.0		V
			V_{OUT} Low		0.15	0.4	
SR	Slew Rate	$V_O = 1.5V$ to 3.5V			175		V/µs
BW	Small-Signal Bandwidth	$A_V = 10$			30		MHz
I_S	Supply Current				12	15	mA
	Shutdown Supply Current	Pin 5 at V^-			0.8	1.5	mA
$I_{S/D}$	Shutdown Pin Current	Pin 5 at V^-			5	25	µA

±5V ELECTRICAL CHARACTERISTICS $-55°C \leq T_A \leq 125°C$, (Note 3)

$V_S = \pm5V$, $V_{REF} = 0V$, $R_{FB1} = 900\Omega$ from pins 6 to 8, $R_{FB2} = 100\Omega$ from pin 8 to ground, $R_L = R_{FB1} + R_{FB2} = 1k$, $C_L \leq 10pF$, pin 5 open.

SYMBOL	PARAMETER	CONDITIONS	LT1189M MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	Either Input, (Note 4)		1.0	7.5	mV
$\Delta V_{OS}/\Delta T$	Input V_{OS} Drift			10		µV/°C
I_{OS}	Input Offset Current	Either Input		0.2	1.5	µA
I_B	Input Bias Current	Either Input		±0.5	±3.5	µA
	Input Voltage Range		–2.5		3.5	V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = -2.5V$ to 3.5V	80	105		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm2.375V$ to ±8V	65	90		dB
V_{OUT}	Output Voltage Swing	$V_S = \pm5V$, $R_L = 1k$, $A_V = 50$	±3.7	±4.0		V
		$V_S = \pm8V$, $R_L = 1k$, $A_V = 50$	±6.6	±7.0		
		$V_S = \pm8V$, $R_L = 300\Omega$, $A_V = 50$, (Note 3)	±6.4	±6.6		
G_E	Gain Error	$V_O = \pm1V$, $A_V = 10$, $R_L = 1k$		1.0	6.0	%
I_S	Supply Current			13	17	mA
	Shutdown Supply Current	Pin 5 at V^-, (Note 11)		0.8	1.5	mA
$I_{S/D}$	Shutdown Pin Current	Pin 5 at V^-		5	25	µA

±5V ELECTRICAL CHARACTERISTICS

$0°C \le T_A \le 70°C$, (Note 3)

$V_S = \pm5V$, $V_{REF} = 0V$, $R_{FB1} = 900\Omega$ from pins 6 to 8, $R_{FB2} = 100\Omega$ from pin 8 to ground, $R_L = R_{FB1} + R_{FB2} = 1k$, $C_L \le 10pF$, pin 5 open.

SYMBOL	PARAMETER	CONDITIONS	LT1189C MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage (Note 4)	Either Input SOIC Package		1.0 1.0	3.0 6.0	mV mV
$\Delta V_{OS}/\Delta T$	Input V_{OS} Drift			5.0		µV/°C
I_{OS}	Input Offset Current	Either Input		0.2	1.5	µA
I_B	Input Bias Current	Either Input		±0.5	±3.5	µA
	Input Voltage Range		–2.5		3.5	V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = -2.5V$ to 3.5V	80	105		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm2.375V$ to ±8V	70	90		dB
V_{OUT}	Output Voltage Swing	$V_S = \pm5V$, $R_L = 1k$, $A_V = 50$	±3.7	±4.0		V
		$V_S = \pm8V$, $R_L = 1k$, $A_V = 50$	±6.6	±7.0		
		$V_S = \pm8V$, $R_L = 300\Omega$, $A_V = 50$, (Note 3)	±6.4	±6.6		
G_E	Gain Error	$V_O = \pm1V$, $A_V = 10$, $R_L = 1k$		1.0	3.5	%
I_S	Supply Current			13	17	mA
	Shutdown Supply Current	Pin 5 at V^-, (Note 11)		0.8	1.5	mA
$I_{S/D}$	Shutdown Pin Current	Pin 5 at V^-		5	25	µA

5V ELECTRICAL CHARACTERISTICS

$0°C \le T_A \le 70°C$, (Note 3)

$V_S^+ = +5V$, $V_S^- = 0V$, $V_{REF} = 2.5V$, $R_{FB1} = 900\Omega$ from pins 6 to 8, $R_{FB2} = 100\Omega$ from pin 8 to V_{REF}, $R_L = R_{FB1} + R_{FB2} = 1k$, $C_L \le 10pF$, pin 5 open.

SYMBOL	PARAMETER	CONDITIONS		LT1189C MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage, (Note 4)	Either Input			1.0	3.0	mV
$\Delta V_{OS}/\Delta T$	Input V_{OS} Drift				5.0		µV/°C
I_{OS}	Input Offset Current	Either Input			0.2	1.5	µA
I_B	Input Bias Current	Either Input			±0.5	±3.5	µA
	Input Voltage Range			2.0		3.5	V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = 2.0V$ to 3.5V		80	100		dB
V_{OUT}	Output Voltage Swing	$R_L = 300\Omega$ to Ground	V_{OUT} High	3.5	4.0		V
		(Note 3)	V_{OUT} Low		0.15	0.4	
I_S	Supply Current				12	16	mA
	Shutdown Supply Current	Pin 5 at V, (Note 11)			0.8	1.5	mA
$I_{S/D}$	Shutdown Pin Current	Pin 5 at V^-			5	25	µA

Note 1: A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted continuously.

Note 2: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formulas:

LT1189MJ8, LT1189CJ8: $T_J = T_A + (P_D \times 100°C/W)$
LT1189CN8: $T_J = T_A + (P_D \times 100°C/W)$
LT1189CS8: $T_J = T_A + (P_D \times 150°C/W)$

Note 3: When $R_L = 1k$ is specified, the load resistor is $R_{FB1} + R_{FB2}$, but when $R_L = 300\Omega$ is specified, then an additional 430Ω is added to the output such that ($R_{FB1} + R_{FB2}$) in parallel with 430Ω is $R_L = 300\Omega$.

Note 4: V_{OS} measured at the output (pin 6) is the contribution from both input pair, and is input referred.

Note 5: $V_{IN\ LIM}$ is the maximum voltage between $-V_{IN}$ and $+V_{IN}$ (pin 2 and pin 3) for which the output can respond.

Note 6: Slew rate is measured between ±1V on the output, with a V_{IN} step of ±0.5V, $A_V = 10$ and $R_L = 1k$.

Note 7: Full power bandwidth is calculated from the slew rate measurement: $FPBW = SR/2\pi Vp$.

Note 8: Settling time measurement techniques are shown in "Take the Guesswork Out of Settling Time Measurements," EDN, September 19, 1985.

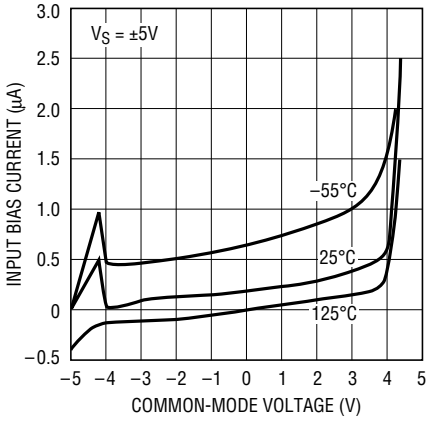
Note 9: NTSC (3.58MHz).

Note 10: AC parameters are 100% tested on the ceramic and plastic DIP packaged parts (J8 and N8 suffix) and are sample tested on every lot of the SO packaged parts (S8 suffix).

Note 11: See Application section for shutdown at elevated temperatures. Do not operate shutdown above $T_J > 125°C$.

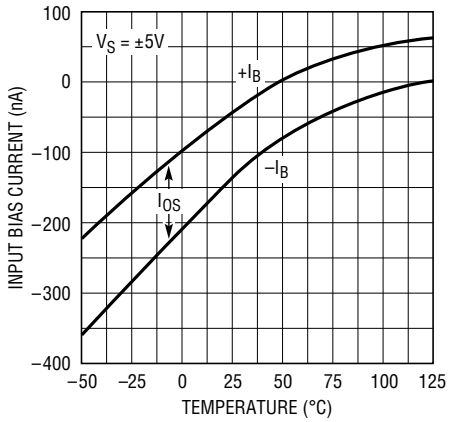
TYPICAL PERFORMANCE CHARACTERISTICS

Input Bias Current vs Common-Mode Voltage



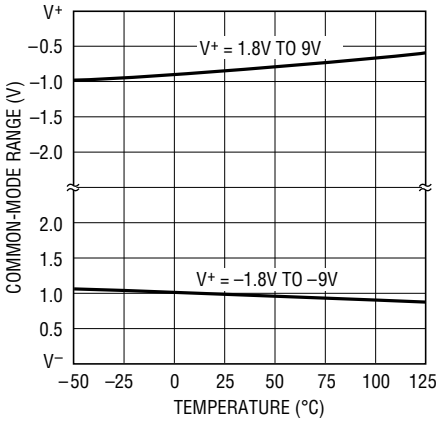
LT1189 • TPC01

Input Bias Current vs Temperature



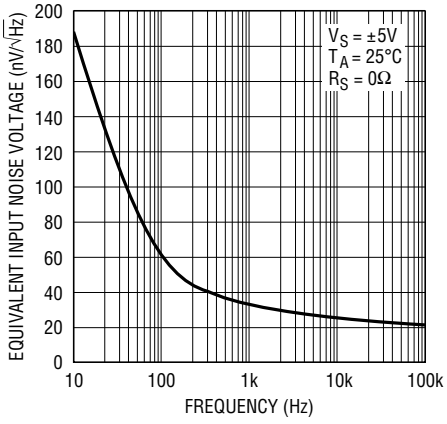
LT1189 • TPC02

Common-Mode Voltage vs Temperature



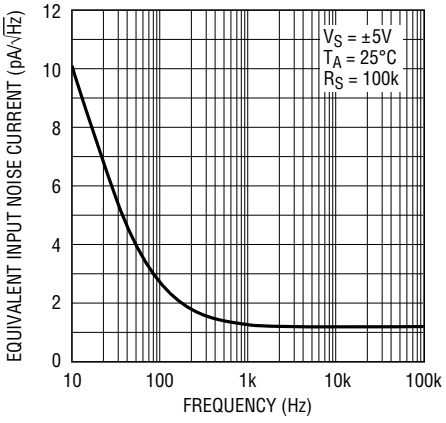
LT1189 • TPC03

Equivalent Input Noise Voltage vs Frequency



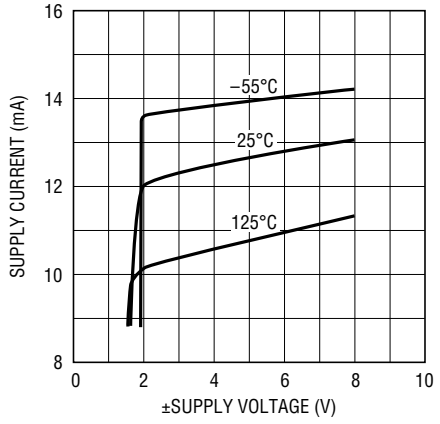
LT1189 • TPC04

Equivalent Input Noise Current vs Frequency



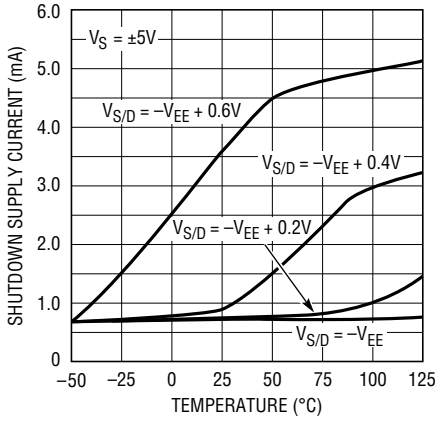
LT1189 • TPC05

Supply Current vs Supply Voltage



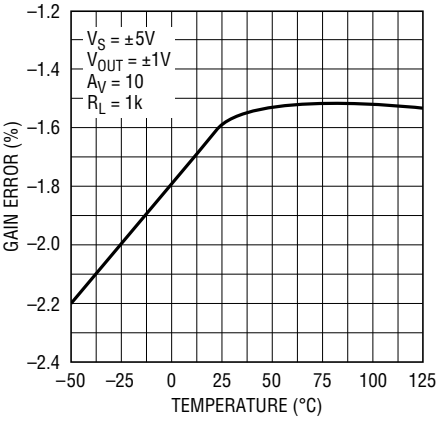
LT1189 • TPC06

Shutdown Supply Current vs Temperature



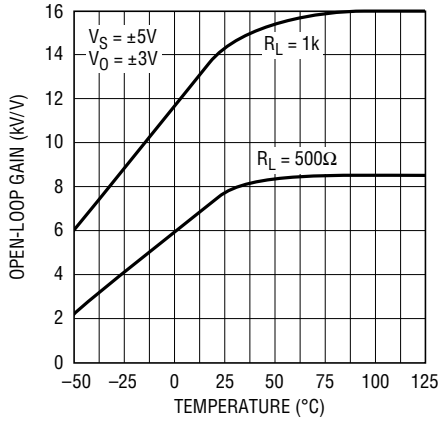
LT1189 • TPC07

Gain Error vs Temperature



LT1189 • TPC08

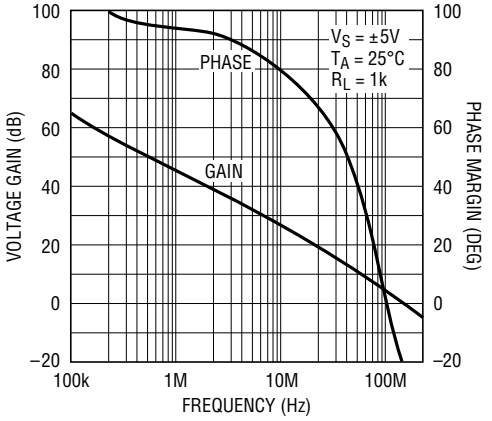
Open-Loop Gain vs Temperature



LT1189 • TPC09

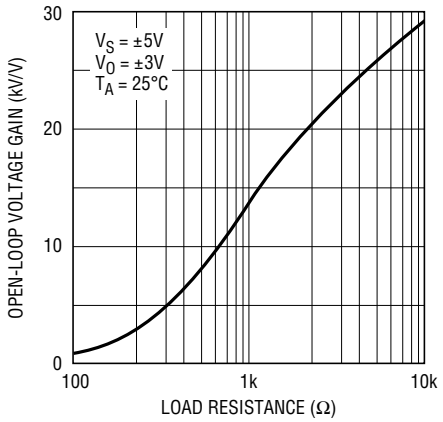
TYPICAL PERFORMANCE CHARACTERISTICS

Gain, Phase vs Frequency



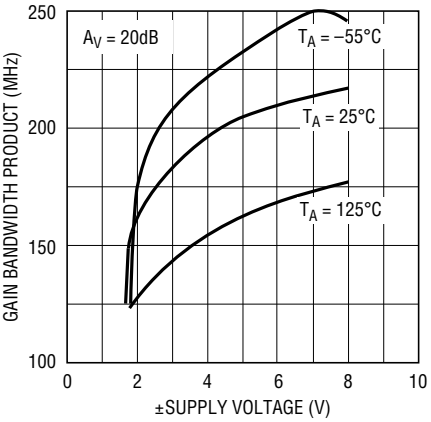
LT1189 • TPC11

Open-Loop Voltage Gain vs Load Resistance



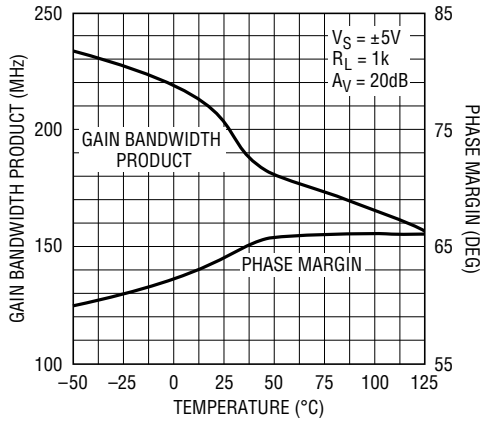
LT1189• TPC10

Gain Bandwidth Product vs Supply Voltage



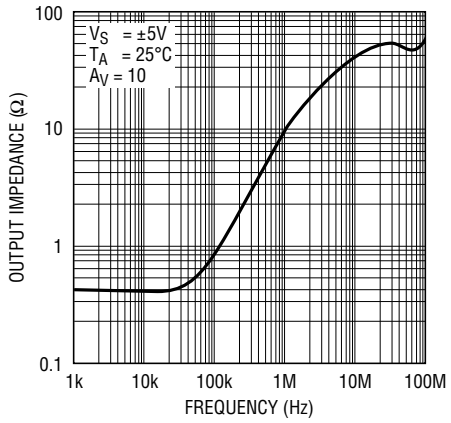
LT1189 • TPC12

Gain Bandwidth Product and Phase Margin vs Temperature



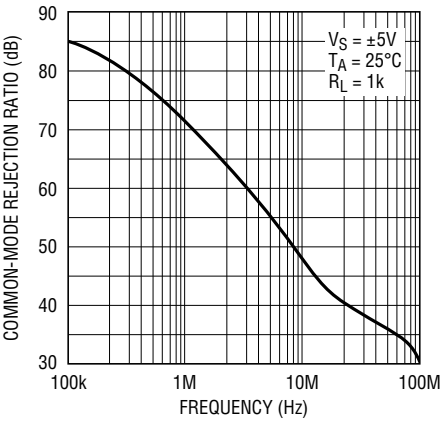
LT1189 • TPC13

Output Impedance vs Frequency



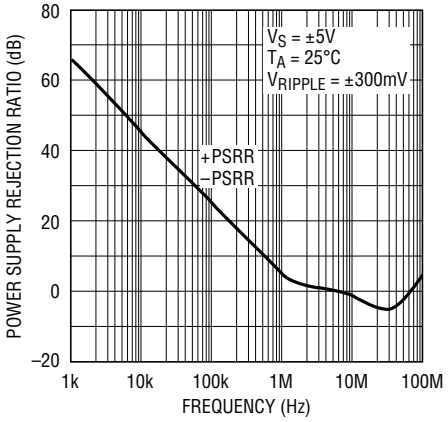
LT1189 • TPC14

Common-Mode Rejection Ratio vs Frequency



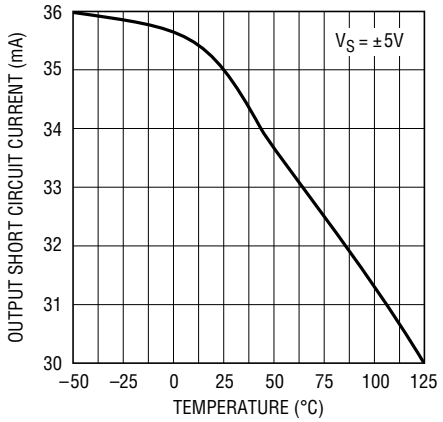
LT1189 • TPC15

Power Supply Rejection Ratio vs Frequency



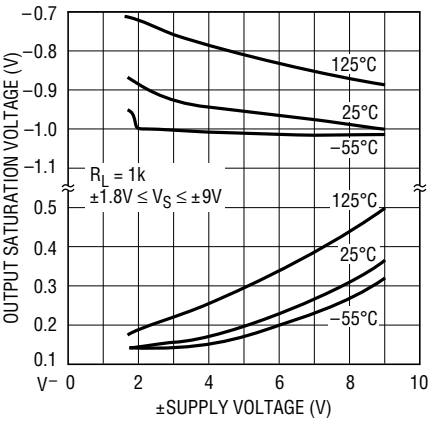
LT1189 • TPC16

Output Short Circuit Current vs Temperature



LT1189 • TPC17

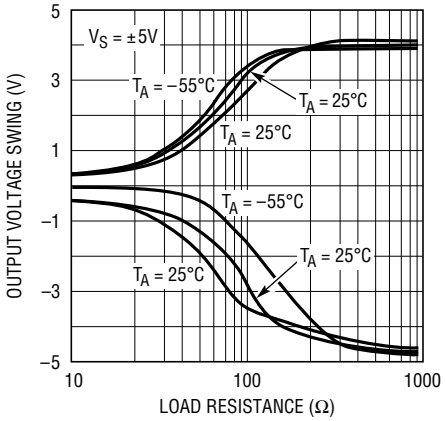
± Output Swing vs Supply Voltage



LT1189 • TPC18

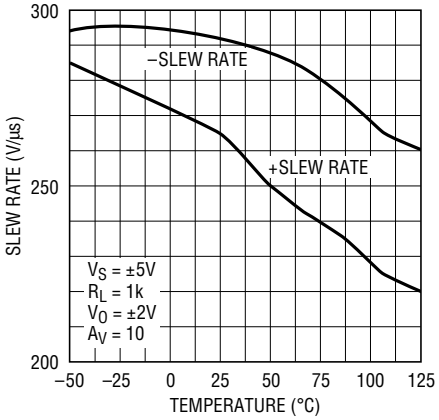
TYPICAL PERFORMANCE CHARACTERISTICS

Output Voltage Swing vs Load Resistance



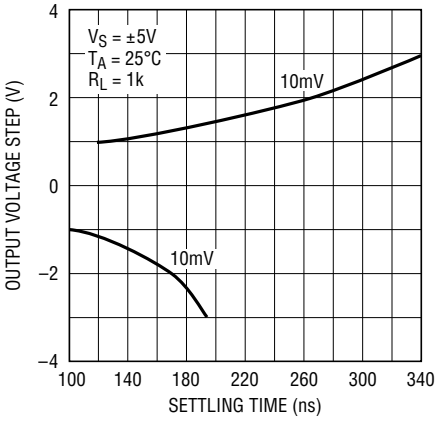
LT1189 • TPC19

Slew Rate vs Temperature



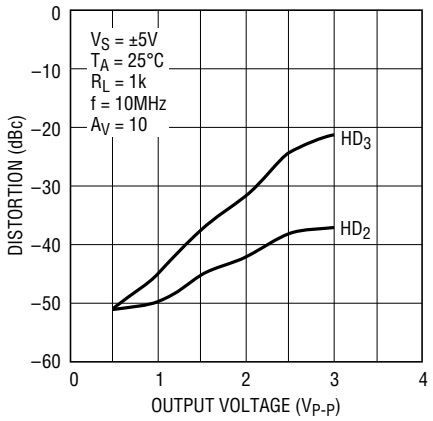
LT1189 • TPC20

Output Voltage Step vs Settling Time, A_V = 10



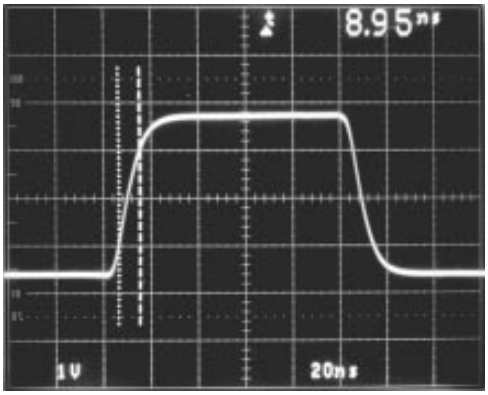
LT1189 • TPC21

Harmonic Distortion vs Output Level



LT1189 • TPC22

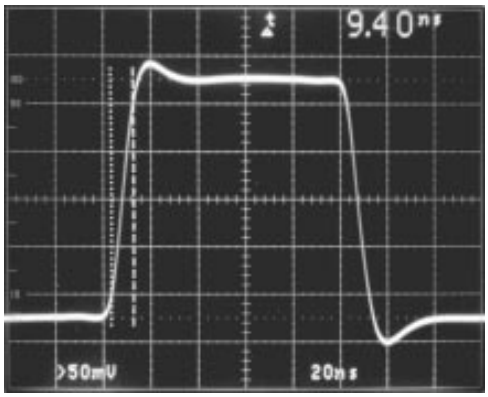
Large-Signal Transient Reponse



A_V = 10, R_L = 1k, +SR = 223V/µs, –SR = 232V/µs

LT1189 • TPC23

Small-Signal Transient Reponse



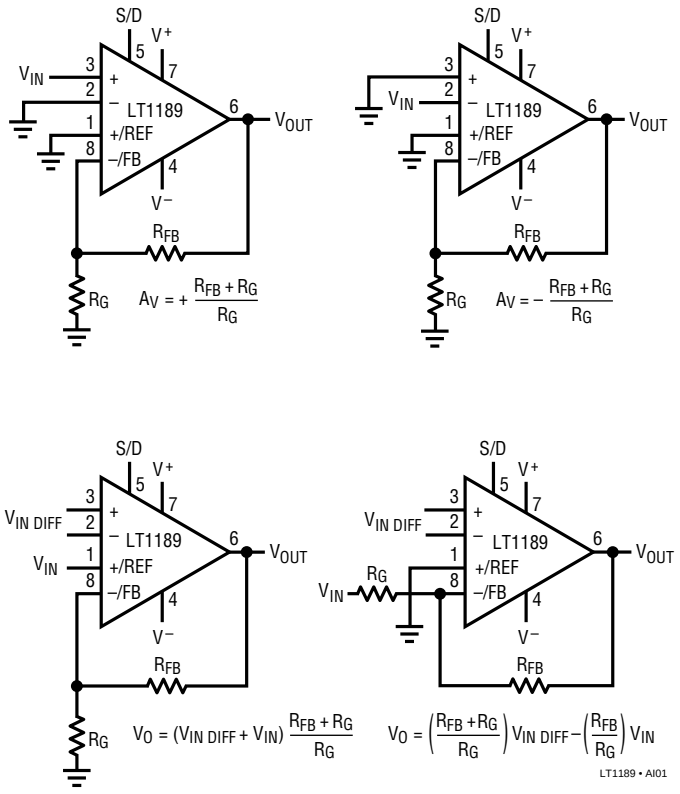
A_V = 10, R_L = 1k, t_r = 9.40ns

LT1189 • TPC24

APPLICATIONS INFORMATION

The primary use of the LT1189 is in converting high speed differential signals to a single-ended output. The LT1189 video difference amplifier has two uncommitted high input impedance (+) and (–) inputs. The amplifier has another set of inputs which can be used for reference and feedback. Additionally, this set of inputs give gain adjust, and DC control to the differential amplifier. The voltage gain of the LT1189 is set like a conventional operational amplifier. Feedback is applied to pin 8, and it is optimized for gains of 10 or greater. The amplifier can be operated single-ended by connecting either the (+) or (–) inputs to the +/REF (pin 1). The voltage gain is set by the resistors: $(R_{FB} + R_G)/R_G$.

Like the single-ended case, the differential voltage gain is set by the external resistors: $(R_{FB} + R_G)/R_G$. The maximum input differential signal for which the output will respond is approximately ±170mV.



Power Supply Bypassing

The LT1189 is quite tolerant of power supply bypassing. In some applications a 0.1µF ceramic disc capacitor placed 1/2 inch from the amplifier is all that is required. In applications requiring good settling time, it is important to use multiple bypass capacitors. A 0.1µF ceramic disc in parallel with a 4.7µF tantalum is recommended.

Calculating the Output Offset Voltage

Both input stages contribute to the output offset voltage at pin 6. The feedback correction forces balance in the input stages by introducing an Input V_{OS} at pin 8. The complete expression for the output offset voltage is:

$$V_{OUT} = (V_{OS} + I_{OS}(R_S) + I_B(R_{REF})) \times (R_{FB} + R_G)/R_G + I_B(R_{FB})$$

R_S represents the input source resistance, typically 75Ω, and R_{REF} represents finite source impedance from the DC reference voltage, for V_{REF} grounded, R_{REF} = 0Ω the I_{OS} is normally a small contributor and the expression simplifies to:

$$V_{OUT} = V_{OS}(R_{FB} + R_G)/R_G + I_B(R_{FB})$$

If R_{FB} is limited to 1k, the last term of the equation contributes only 2mV since I_B is less than 2µA.

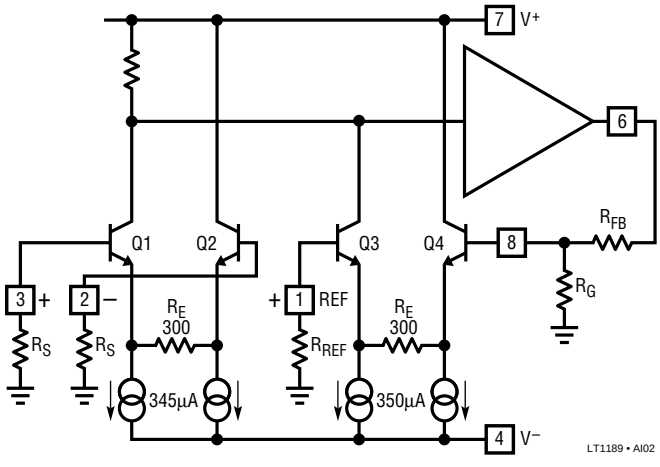


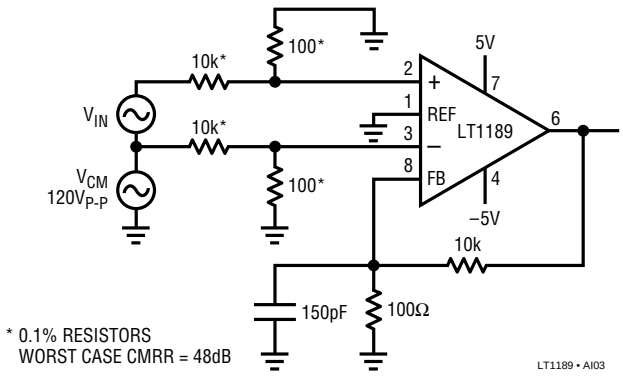
Figure 1. Simplified Input Stage Schematic

APPLICATIONS INFORMATION

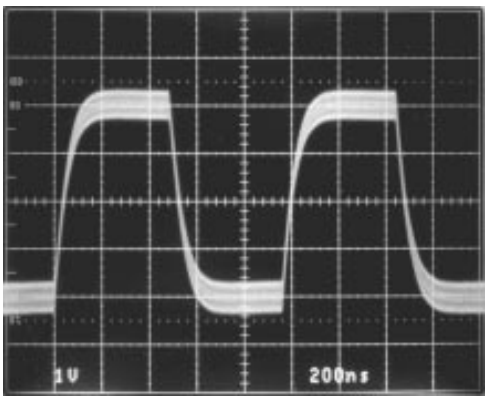
Instrumentation Amplifier Rejects High Voltage

Instrumentation amplifiers are often used to process slowly varying outputs from transducers. With the LT1189 it is easy to make an instrumentation amplifier that can respond to rapidly varying signals. Attenuation resistors in front of the LT1189 allow very large common-mode signals to be rejected while maintaining good frequency response. The input common-mode and differential-mode signals are reduced by 100:1, while the closed-loop gain is set to be 100, thereby maintaining unity-gain input to output. The unique topology allows for frequency response boost by adding 150pF to pin 8 as shown.

3.5MHz Instrumentation Amplifier Rejects 120V$_{P-P}$

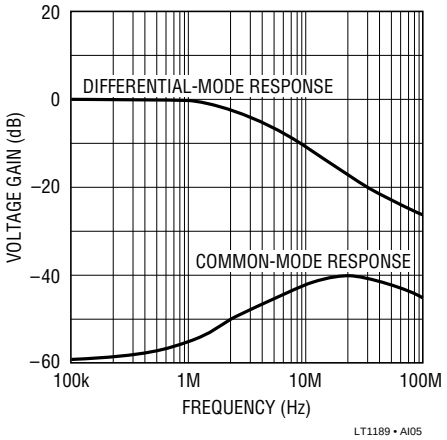


Output of Instrumentation Amplifier with 1MHz Square Wave Riding on 120V$_{P-P}$ at the Input



LT1189 • AI04

High Voltage Instrumentation Amplifier Response



Operating with Low Closed-Loop Gain

The LT1189 has been optimized for closed-loop gains of 10 or greater. The amplifier can be operated at much lower closed-loop gains with the aid of a capacitor C_{FB} across the feedback resistor, (feedback zero). This capacitor lowers the closed-loop 3dB bandwidth. The bandwidth cannot be made arbitrarily low because C_{FB} is a short at high frequency and the amplifier will appear configured unity-gain. As an approximate guideline, make $BW \times A_{VCL}$ = 200MHz. This expression expands to:

$$\frac{A_{VCL}}{2\pi(R_{FB})(C_{FB})} = 200MHz$$

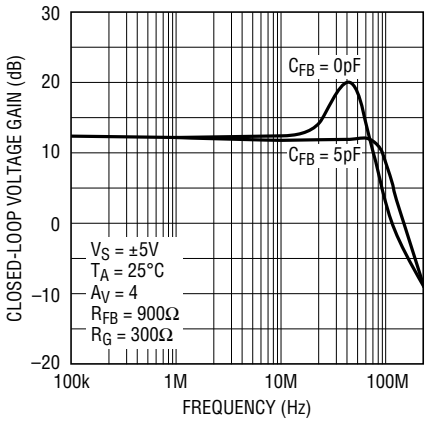
or:

$$C_{FB} = \frac{A_{VCL}}{(200MHz)(2\pi)(R_{FB})}$$

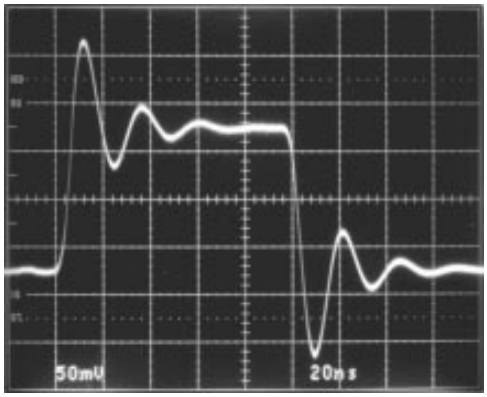
The effect of the feedback zero on the transient and frequency response is shown for A_V = 4.

APPLICATIONS INFORMATION

Closed-Loop Voltage Gain vs Frequency



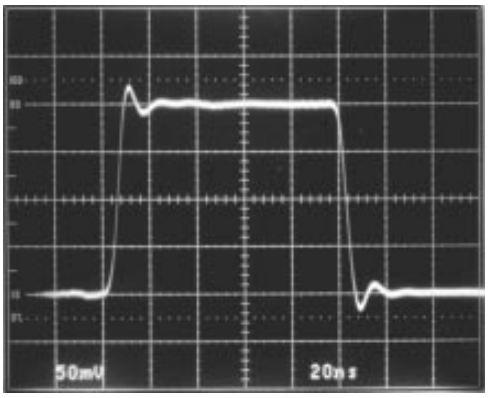
Small-Signal Transient Response



A_V = 4, R_{FB} = 910Ω, R_G = 300Ω

LT1189 • AI07

Small-Signal Transient Response



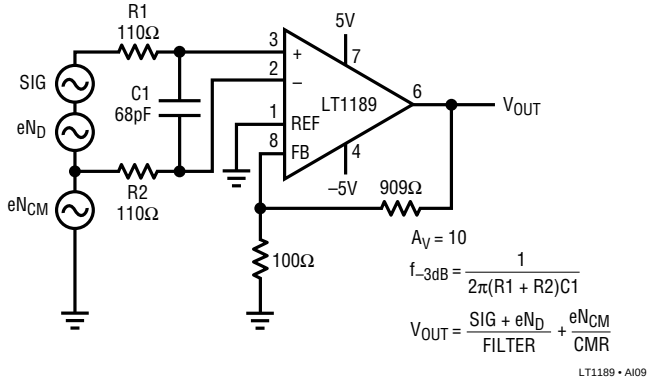
A_V = 4, R_{FB} = 910Ω, R_G = 300Ω, CFB = 5pF

LT1189 • AI08

Reducing the Closed-Loop Bandwidth

Although it is possible to reduce the closed-loop bandwidth by using a feedback zero, instability can occur if the bandwidth is made too low. An alternate technique is to do differential filtering at the input of the amplifier. This technique filters the differential input signal, and the differential noise, but does not filter common-mode noise. Common-mode noise is rejected by the LT1189's CMRR.

10MHz Bandwidth Limited Amplifier

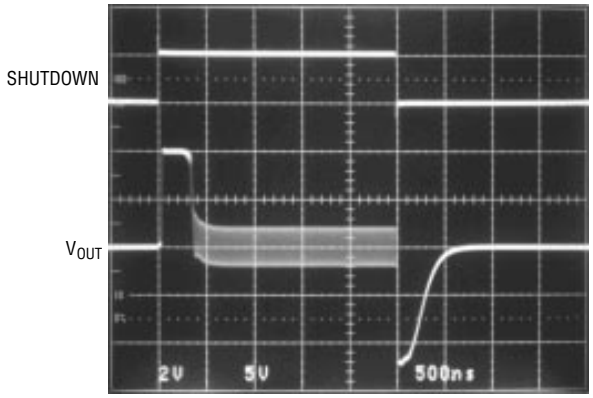


Using the Shutdown Feature

The LT1189 has a unique feature that allows the amplifier to be shutdown for conserving power, or for multiplexing several amplifiers onto a common cable. The amplifier will shutdown by taking pin 5 to V^-. In shutdown, the amplifier dissipates 15mW while maintaining a true high impedance output state of about 20kΩ in parallel with the feedback resistors. For MUX applications, the amplifiers may be configured inverting, non-inverting, or differential. When the output is loaded with as little as 1kΩ from the amplifier's feedback resistors, the amplifier shuts off in 600ns. This shutoff can be under the control of HC CMOS operating between 0V and –5V.

APPLICATIONS INFORMATION

1MHz Sine Wave Gated Off with Shutdown Pin



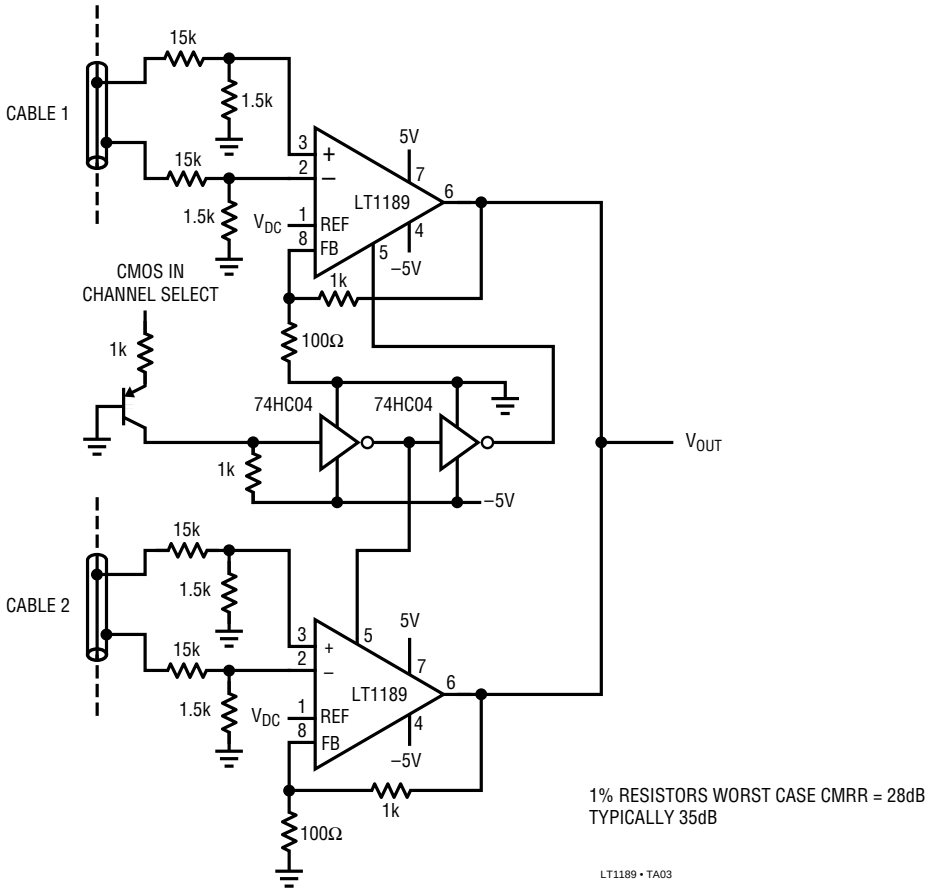
A_V = 10, R_{FB} = 900Ω, R_G = 100Ω

LT1189 • AI10

The ability to maintain shutoff is shown on the curve Shut down Supply Current vs Temperature in the Typical Performance Characteristics section. At very high elevated temperature it is important to hold the shutdown pin close to the negative supply to keep the supply current from increasing.

TYPICAL APPLICATION

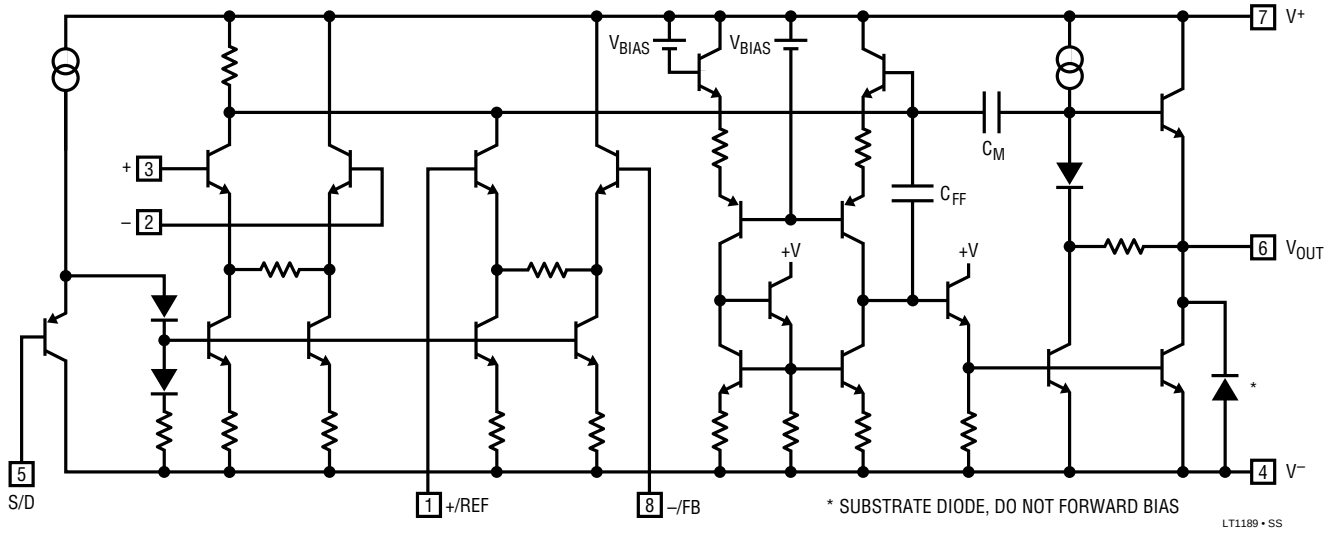
Differential Receiver MUX for Power Down Applications



1% RESISTORS WORST CASE CMRR = 28dB
TYPICALLY 35dB

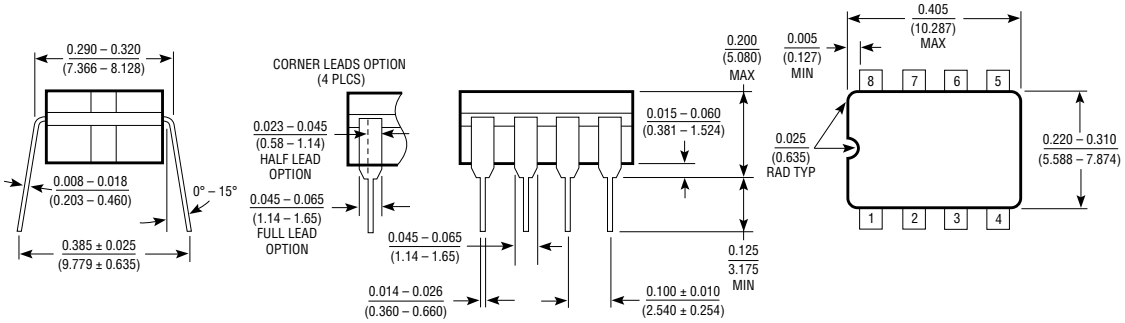
LT1189 • TA03

SIMPLIFIED SCHEMATIC

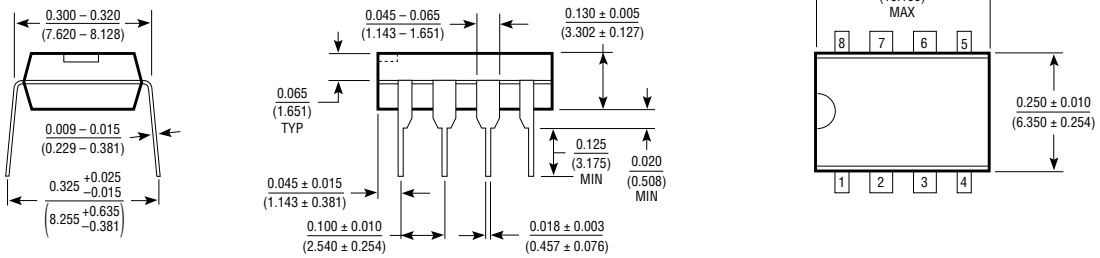


PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

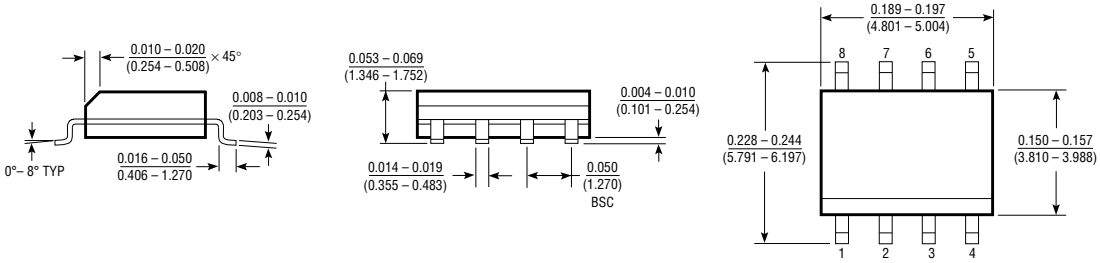
J8 Package
8-Lead Hermetic DIP



N8 Package
8-Lead Plastic DIP



S8 Package
8-Lead Plastic SOIC



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