SPECTRUM DIGITAL INCORPORATED

TMS320DM365 Evaluation Module

Technical Reference

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About This Manual

This document describes the board level operations of the DM365 Evaluation Module (EVM). The EVM is based on the Texas Instruments TMS320DM365 Processor.

The DM365 Evaluation Module is a table top card that allows engineers and software developers to evaluate certain characteristics of the DM365 processor to determine if the processor meets the designers application requirements. Evaluators can create software to execute on board or expand the system in a variety of ways.

Notational Conventions

This document uses the following conventions.

The DM365 Evaluation Module will sometimes be referred to as the DM365 EVM or EVM.

Program listings, program examples, and interactive displays are shown in a special italic typeface. Here is a sample program listing.

equations
!rd = !strobe&rw;

Information About Cautions

This book may contain cautions.
This is an example of a caution statement.
A caution statement describes a situation that could potentially damage your software, or hardware, or other equipment. The information in a caution is provided for your protection. Please read each caution carefully.

Related Documents, Application Notes and User Guides

Information regarding the TMS320DM365 can be found at the following Texas Instruments website:

http://www.ti.com

Table 1: Manual History

Revision	History
A	Beta Release

Table 2: Board History

PWB Revision	History
C	Beta Release

Chapter 1

Introduction to the DM365 EVM

Chapter One provides a description of the DM365 EVM along with the key features and a block diagram of the circuit board.

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1.1 Key Features

The DM365 EVM is a standalone development platform that enables users to evaluate and develop applications for the TMS320DM365 processor. Schematics, logic equations and application notes are available to ease hardware development and reduce time to market.

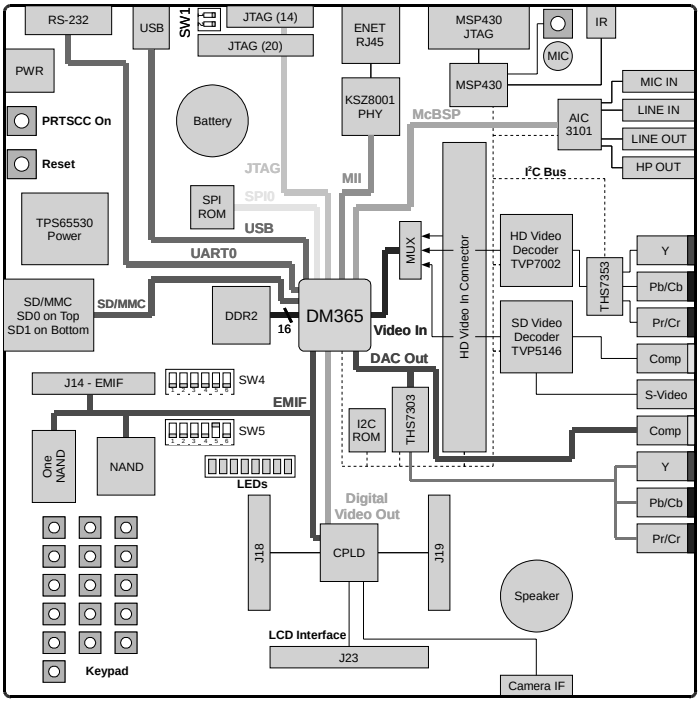

Figure 1-1, Block Diagram DM365 EVM

The EVM comes with a full complement of on board devices that suit a wide variety of application environments. Key features include:

- A Texas Instruments DM365 processor with an ARM9 processor operating up to 300 MHz.
- 1 video input port, supports composite or S video (NTSC or PAL formats)
- 1 set of 3 component video inputs supports capture up to 720P resolution
- 1 composite video DAC output (NTSC or PAL formats)
- 1 set of 3 component video DACs supports resolution up to 720P resolution
- 128 Mbytes of DDR2 DRAM
- UART Interface
- Dual SD/MMC/MS, MMC/SD Media Card Interfaces

- 2 Gigabytes NAND Flash
- 128 Megabytes of One NAND
- AIC3101 stereo codec
- USB2 Interface
- 10/100 MBS RMII Ethernet Interface
- SPI EEPROM
- IR Remote Interface via MSP430
- Configurable boot load options
- 8 user LEDs/16 user push button switches
- Single voltage power supply (+5V)
- Expansion connectors for daughter card use
- 14 Pin TI JTAG/20 Pin ARM JTAG Interfaces

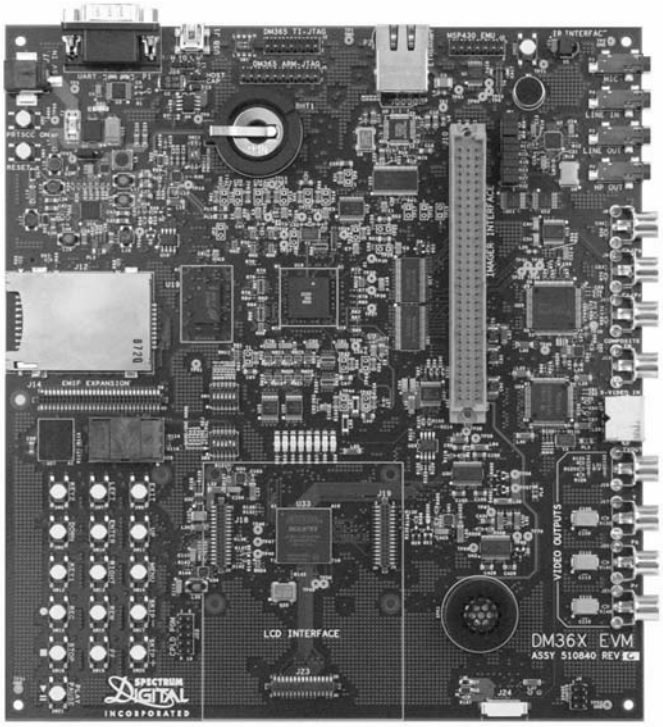

Figure 1-2, DM365 EVM

1.2 Functional Overview of the DM365 EVM

The DM365 on the EVM interfaces to on-board peripherals through the 8/16-bit wide Async EMIF peripheral interface pins. The DDR2 memory is connected to its own dedicated 16 bit wide bus. The Async EMIF bus is also connected to the NAND and One NAND flash.

On board video decoders and on chip encoders interface video streams to the DM365 processor. One composite channel and one set of 3 component channel encoder/decoder are standard on the EVM. On screen display functions are implemented in software on the DM365 processor.

An on-board AIC3101 codec allows the DSP to transmit and receive analog audio signals. The I^2C bus is used for the codec control interface, while the McBSP controls the audio stream. Signal interfacing is done through 3.5mm audio jacks that correspond to microphone input, headphone output, line input, and line output.

The EVM includes 8 user LEDs, 16 user push button switches, and an IR interface which provide the user with application interaction.

An included +5V external power supply is used to power the board. On-board switching voltage regulators provide the +1.2 to 1.35V CPU core voltage, +3.3V for peripherals and +1.8V for DDR2 memory.

The DM365 EVM has a 10/100 ethernet interface which provides a standard high speed link to other devices.

The on board media card interface allows the user to conveniently load/store data from a variety of standard memory card formats. An on-chip Real Time Clock is integrated into the DM365 for time based applications.

1.3 Basic Operation

The EVM is designed to work with TI's Code Composer Studio IDE™, or standard GDB tool environments. Code Composer communicates with the board through an external JTAG emulator.

1.4 Memory Map

The DM365 processor has a byte addressable address space. There are some limitations to byte addressing which are determined by peripheral interconnection to the DM365 device. Program code and data can be placed anywhere in the unified address space. Addresses are multiple sizes depending on hardware implementation. Refer to the appropriate device data sheets for more details.

The memory map shows the address space of a generic DM365 processor on the left with specific details of how each region is used on the right. By default, the internal memory sits at the beginning of the address space. Portions of memory can be remapped in software as L2 cache rather than fixed RAM.

The part incorporates a dual EMIF interface. One dedicated EMIF directly interfaces to the DDR2 memory. The other EMIF has 2 separate addressable regions called chip enable spaces (CE0 & CE1). The NAND Flash, one NAND, and CPLD are mapped into these chip enable spaces.

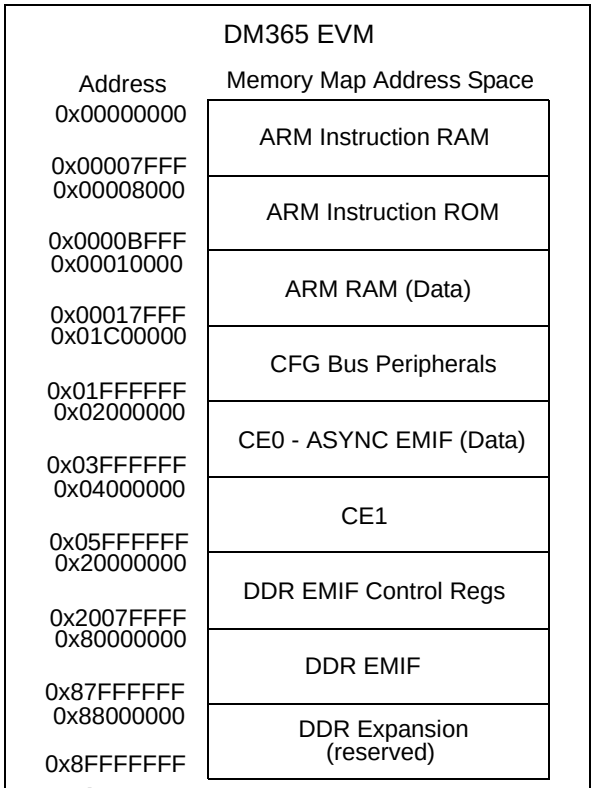

Figure 1-3, Memory Map, DM365 EVM

Shown below is a break out of the memory spaces.

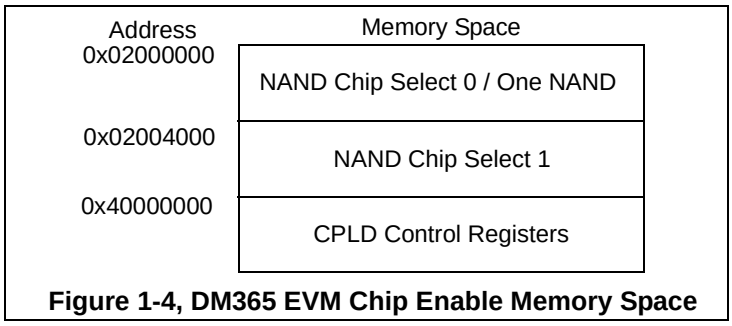

Figure 1-4, DM365 EVM Chip Enable Memory Space

1.5 Boot / Configuration Switch Settings

The EVM has a configuration switch that allow users to control the Boot and EMIF configuration state of the processor when it is released from reset. The switch SW4 determines the source for processor booting. By default the switches are configured to NAND Flash boot. The EMIF configuration switch must be set accordingly. This switch configures the DM365 pin muxing at RESET. The default for the pin muxing is shown below. For additional pin muxing requirements please refer to the D365 data sheet.

Table 1: SW4, ARM Boot Mode Select

Pos 3	Pos 2	Pos 1	HW Code	Boot Mode
ON	ON	ON	0 0 0	NAND Boot *****
ON	ON	OFF	0 0 1	ASYNC EMIF
ON	OFF	ON	0 1 0	MMC/SD Boot
ON	OFF	OFF	0 1 1	UART Boot
OFF	ON	ON	1 0 0	USB Boot
OFF	ON	OFF	1 0 1	SPI Boot
OFF	OFF	ON	1 1 0	EMAC Boot
OFF	OFF	OFF	1 1 1	HPI Boot

Table 2: SW4, ARM EMIF Configuration Mode Select

Pos 6	Pos 5	Pos 4	HW Code	Configuration Mode
ON	ON	ON	0 0 0	8-bit AEMIF Configuration *
ON	ON	OFF	0 0 1	16-bit AEMIF Configuration

***** default setting

1.6 Power Supply

The EVM operates from a single +5V external power supply connected to the main power input (J7), a 2.5 MM. barrel-type plug. Internally, the +5V input is converted into +1.2 to 1.35V, +1.8V and +3.3V using Texas Instruments TPS65530 power management IC and various linear regulators. The +1.2 to 1.35V supply is used for the DSP core while the +3.3V supply is used for the DSP's I/O buffers and other chips on the board. The +1.8 volt supply is used for DM365 DDR2 memory, and other on chip peripherals.

Chapter 2

Board Components

This chapter describes the operation of the major board components on the DM365 EVM.

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2.1 Asynchronous EMIF Interface

An asynchronous 16 bit EMIF with two chip enables divide up the address space and allow for asynchronous accesses on the EVM. This interface connects to the NAND, One NAND, and CPLD registers on the EVM board.

2.1.1 NAND Flash

The DM365 has 2 gigabytes of NAND Flash memory mapped into the CE0 space. The NAND Flash memory is used primarily for boot loading and file system on the DM365 EVM. The CE0 selects the device and needs to be configured to 8 bits wide when accessing the NAND.

Switch SW5, position 1 (OFF) selects CE0 mapped to NAND. The NAND and One NAND interface share the same CE0 chip select so only 1 device can be operational at any given time.

When the NAND flash interface is selected the spare address lines can be used by the internal DM365 key pad interface. This interface is enabled by setting a control bit in the CPLD to enable the on board CBTLV switches to the keypad matrix.

2.1.1.1 One NAND

The EVM supports 128 Megabytes of One NAND. This interface is 16 bits wide and CE0 must be configured for 16 bit wide operation when using One NAND. Switch SW5, position 1 (ON) selects the One NAND device. When the One NAND is selected the on board NAND is not available. Since the One NAND uses all the asynchronous EMIF address lines the on-chip key pad controller on the DM365 cannot be used when the One NAND is selected.

2.1.1.2 CPLD Interface

The DM365 incorporates an Altera EPM2210, 256 Ball Grid Array(BGA) CPLD. The CPLD incorporates a number of internal registers, glue logic, and I/O multiplexing to allow for a very flexible development platform. The CPLD is accessed via EMIF CE1. The interface is 8 bits wide. All registers show up as 4 mirror images in the memory window due to 32 bit addressing and 8 bit data mapping, that is BA0 and BA1 are not used in the memory decoder for registers.

Address lines A7-A3 and BA0 and BA1 are not used in the decoder so that these lines can be used by the keypad decoder.

The base address of CE1 is 0x0400 0000. Each additional register is accessed on an increment of 0x0000 0008. The addresses are in the following format:
A13, A12, A11, A10, A9, A8, Ax, Ax, Ax, Ax, Ax, A2, A1, Ax, Ax.

The following sections describe the registers and their function. A list of the registers is shown in the table below.

Table 1: CPLD Registers

Reg #	Address A13 - A8	Address A2-A1	Function	R/W
0	0 0 0 0 0 0	0 0	CPLD Version	R
1	0 0 0 0 0 0	0 1	Test Register	R,W
2	0 0 0 0 0 0	1 0	LED Register	R,W
3	0 0 0 0 0 0	1 1	Board Mux Control	R,W
4	0 0 0 0 0 1	0 0	Board Switch Register	R
5	0 0 0 0 0 1	0 1	Power Control Register	R,W
6	0 0 0 0 0 1	1 0	GPIO Video Register	R,W
7	0 0 0 0 0 1	1 1	Media Card Status	R
8	0 0 0 0 1 0	0 0	DILC Output Pin Mapping	R,W
9	0 0 0 0 1 0	0 1	DILC Input Pin Mapping	R
10	0 0 0 0 1 0	1 0	Imager Internal I/O Direction Register 0	R,W
11	0 0 0 0 1 0	1 1	Imager Internal I/O Mux Register 0	R,W
12	0 0 0 0 1 1	0 0	Imager Internal I/O Mux Register 1	R,W
13	0 0 0 0 1 1	0 1	Imager Internal I/O Direction Register 1	R,W
14	0 0 0 0 1 1	1 0	Imager Internal I/O Mux Register 2	R,W
15	0 0 0 0 1 1	1 1	Imager Internal I/O Mux Register 3	R,W
16	0 0 0 1 0 0	0 0	Imager Internal I/O Direction Register 2	R,W
17	0 0 0 1 0 0	0 1	Imager Internal I/O Mux Register 4	R,W
18	0 0 0 1 0 0	1 0	Imager Internal I/O Mux Register 5	R,W
19	0 0 0 1 0 0	1 1	Board RESET Register	R,W
720	1 1 1 1 1 0	0 0	CCD Internal I/O Direction Register 1	R,W
721	1 1 1 1 1 0	0 1	CCD Internal I/O Read/Write Register 1	R,W
722	1 1 1 1 1 0	1 0	CCD Internal I/O Direction Register 2	R,W
723	1 1 1 1 1 0	1 1	CCD Internal I/O Read/Write Register 2	R,W
724	1 1 1 1 1 1	0 0	CCD Internal I/O Direction Register 3	R,W
725	1 1 1 1 1 1	0 1	CCD Internal I/O Read/Write Register 3	R,W

2.1.1.2.1 Register 0, CPLD Version

This read only, 8 bit register, contains the CPLD hardware version for version control. The default value is 0x11.

2.1.1.2.2 Register 1, Test Register

This read only, 8 bit register, has a default value of 0xA5 and can be read and written to test the memory interface.

2.1.1.2.3 Register 2, LED Register

This 8 bit, read/write register controls the user LEDs. A data bit of '0' in each bit location turns on an LED. Similarly a '1' turns off the LED in each bit position.

2.1.1.2.4 Register 3, Board Mux Control Register

This 8 bit, read/write control register (default = 0x00) controls keypad, AIC, SD, Ethernet, and Video In multiplexers as shown in the table below.

points as shown in the table below.

Table 2: Register 3, Board Mux Control Register

Bit #	Signal	State	Function
7	EMIF_KEYPAD_CTL	0	Addresses on Muxes (ONE NAND Mode)
		1	Addresses are available for keypad
6	SEL_SD1_GPIO_CTL	0	Enables SD card slot 1
		1	Signals for SD1 card slot 1 go to CPLD imager GPIO
5	SEL_AICn_GPIO_CTL	0	Enables McBSP signals to AIC3101 codec
		1	McBSP signals go to CPLD for imager GPIO
4	Spare		Not currently used
3	SEL_ENET_GPIO_CTL	0	Enable Ethernet signals to PHY
		1	Ethernet signals go to CPLD for imager GPIO
2	DECODER_IMAGER_S2_CTL	S[2:0]	0 0 1 = Selects TVP7002 as input to DM365 video input port 0 1 0 = Selects imager as input to DM365 video input port 1 0 1 = Selects TVP5146 as input to DM365 video input port
1	DECODER_IMAGER_S1_CTL		
0	DECODER_IMAGER_S0_CTL		

2.1.1.2.5 Register 4, Board Switch Register

This 8 bit, read only register mirrors the values set on switch SW5. These signals are shown in the table below.

Table 3: Register 4, Board Switch Register

Bit #	SW5 Position	Signal
7	Reserved	N/A
6	Reserved	N/A
5	1	SEL_NAND_LOW 0 = NAND mapped to CE0, 1 = ONE NAND mapped to CE0
4	2	SEL_EXTRA1
3	3	SEL_EXTRA2
2	4	SEL_EXTRA3
1	5	CPU_VSEL1 0 = Vcore at 1.2V 1 = Vcore at 1.35 V
0	6	SEL_NTAS_MODE

2.1.1.2.6 Register 5, Power Control Register

Register 5 is a 8 bit, read/write register that controls on board voltage regulator functions. The default data value is 0b00000000. These controls are shown in the table below.

Table 4: Register 5, Power Control Register

Bit #	Signal	Function
7	LCD_OE_5V	0,1 = Sets U32 FDC6331L Pin to 0,1
6	ENABLE_LCD_3V3	0 = Disables U31 TPS74701 1 = Enables U31 TPS74701
5	Reserved	
4	EN7	0,1 = Sets U14 TPS65530 EN7 pin to 0,1
3	ENAFE	0,1 = Sets U14 TPS65530 ENAFE pin to 0,1
2	SEQ56	0,1 = Sets U14 TPS65530 SEQ56 pin to 0,1
1	EN56	0,1 = Sets U14 TPS65530 EN56 pin to 0,1
0	ENABLE_LCD_15V	0 = Disables U34 TPS61080 register 0 = Enables U34 TPS61080 register

2.1.1.2.7 Register 6, GPIO Video Register

Register 6 is a 8 bit, read/write register that controls the mapping of GPIO30/32/33, VDIN_WE, DRV_BUS. The default data value is 0b00000000. These controls are shown in the table below.

Table 5: Register 6, GPIO Video Register

Bit #	Signal	Function
7	Reserved	
6	Reserved	
5	C_FIELD	1 = DM365 Ball E13 mapped to EXP CONN CCD_FIELD
4	C_WE	1 = DM365 Ball E13 mapped to EXP CONN CCD_WEN
3	24 BIT COLOR	1 = Map GPIO30,32,33 to G1,R0,R1 on LCD EXP CONNS
2	C_WE_FLD_VBUS_DRV	1 = DM365 BALL E13 Drives U4, TPS2065
1	GIO33_VBUS_DRV	1 = GIO33 drives U4, TPS2065
0	VBUS_DRV_ALT	1 = Drives VBUS ENABLE to U4, TPS2065

ENABLE VBUS_DRV (U4, TPS2065) will = 1 when any of the following occur:

- When SW5-2 (SEL_EXTRA1_ = 1 for test
- When VBUS_DRV_ALT = 1

ENABLE VBUS_DRV (U4, TPS2065) will = DM365 GIO33 when GIO33_VBUS_DRV = 1

ENABLE VBUS_DRV (U4, TPS2065) will = DM365 Ball E13 when C_WE_FLD_VBUS_DRV = 1

2.1.1.2.8 Register 7, Media Card Status

Register 7 is a 8 bit, read only register that reads the “Insert” and “Write Protect” status of media cards. These functions of these bits are shown in the table below.

Table 6: Register 7, Media Card Status

Bit #	Signal	Function
7	Reserved	Reads 0
6	Reserved	Reads 0
5	SD_MMC_1 WRITE PROTECT	0 = Write Protect
4	SD_MMC_1 INSERT	0 = Insert
3	Reserved	Reads 0
2	SD_MMC0 MS INSERT	0 = Insert
1	SD_MMC_0 WRITE PROTECT	0 = Write Protect
0	SD_MMC_0 INSERT	0 = Insert

2.1.1.2.9 Register 8, DILC Output Pin Mapping

Register 8 is a 8 bit, read/write register that maps DM365 GPIO and SPI2 pins to the DILC connector. The default data value is 0b11111111. The mapping of these pins is shown in the table below.

Table 7: Register 8, DILC Output Pin Mapping

Bit #	Signal	Function
7	DILC_DRV_VBUS	Register drives DILC DRV_VBUS pin when bit 6 = 0
6	DILC_DRV_VBUS_IO	0 = Internal register bit 7 drives DILC pin
5	DILC_VBUS_DET_DRV	Register drives DILC pin VBUS_DET when bit 4 = 0
4	DILC_VBUS_DET_IO	0 = Internal register bit 5 drives DILC pin
3	Reserved	N/A
2	CPU_GPIO32_IO	0 = IN, SPI2_DILC drives GIO32 1 = OUT, GIO32 drives SPI2_DILC
1	CPU_GPIO31_IO	0 = IN, SPI2_DILC drives GIO31 1 = OUT, GIO31 drives SPI2_DILC
0	CPU_GPIO30_IO	0 = IN, SPI2_DILC drives GIO30 1 = OUT, GIO30 drives SPI2_DILC

2.1.1.2.10 Register 9, DILC Input Pin Mapping

Register 9 is a 8 bit, read only register that maps DILC pins to read contents on this register. The mapping of these pins is shown in the table below.

Table 8: Register 9, DILC Input Pin Mapping

Bit #	Function
7	Reserved
6	Reads value of DILC connector pin GIO_DILC_DRV_VBUS1
5	Reads value of DILC connector pin GIO_DILC_DRV_DET
4	Reserved
3	Reads value of DILC connector pin GIO_DILC_DOCK_DET
2	Reads value of DILC connector pin GIO_DILC_CAM_PWR_DECT
1	Reads value of DILC connector pin GIO_DILC_AVJ_DET
0	Reads value of DILC connector pin GIO_DILC_CHG_CTL

2.1.1.2.11 Register 10, Imager Internal I/O Direction Register 0

Register 10 is a 8 bit, read/write register that controls DM365 GPIO to IMAGER connector pin input/output mapping. The default data value is 0b11111111. This mapping is shown in the table below.

Table 9: Register 10, Imager Internal I/O Direction Register 0

Bit #	Function	Mapping
7	0 = GPIO_MD8 to DM365 pin	0 = Outputs 1 = DM365 pins are inputs
6	0 = GPIO_MD7 to DM365 pin	0 = Outputs 1 = DM365 pins are inputs
5	0 = GPIO_MD6 to DM365 pin	0 = Outputs 1 = DM365 pins are inputs
4	0 = GPIO_MD5 to DM365 pin	0 = Outputs 1 = DM365 pins are inputs
3	0 = GPIO_MD4 to DM365 pin	0 = Outputs 1 = DM365 pins are inputs
2	0 = GPIO_MD3 to DM365 pin	0 = Outputs 1 = DM365 pins are inputs
1	0 = SPI4_SDI_GPIO_MD2 to DM365 pin	0 = Outputs 1 = DM365 pins are inputs
0	0 = GPIO_MD1 to DM365 pin	0 = Outputs 1 = DM365 pins are inputs

2.1.1.2.12 Register 11, Internal I/O Mux Register 0

Register 11 is a 8 bit, read/write register that controls DM365 GPIO Muxing to IMAGER connector pin input. The default data is 0b00000000. The table below shows this muxing.

Table 10: Register 11, Internal I/O Mux Register 0

Bit #	Muxing
7	0 = GPIO_MD4 MUX SELB
6	0 = GPIO_MD4 MUX SELA
5	0 = GPIO_MD3 MUX SELB
4	0 = GPIO_MD3 MUX SELA
3	0 = SPI4_SDI_GPIO_MD2 MUX SELB
2	0 = SPI4_SDI_GPIO_MD2 MUX SELA
1	0 = GPIO_MD1 MUX SELB
0	0 = GPIO_MD1 MUX SELA

2.1.1.2.13 Register 12, Internal I/O Mux Register 1

Register 12 is a 8 bit, read/write register that controls DM365 GPIO Muxing to IMAGER connector pin input. The default data is 0b00000000. The table below shows this muxing.

Table 11: Register 12, Internal I/O Mux Register 1

Bit #	Muxing
7	0 = GPIO_MD8 MUX SELB
6	0 = GPIO_MD8 MUX SELA
5	0 = GPIO_MD7 MUX SELB
4	0 = GPIO_MD7 MUX SELA
3	0 = GPIO_MD6 MUX SELB
2	0 = GPIO_MD6 MUX SELA
1	0 = GPIO_MD5 MUX SELB
0	0 = GPIO_MD5 MUX SELA

2.1.1.2.14 Register 13, Imager Internal I/O Direction Register 1

Register 13 is a 8 bit, read/write register that controls DM365 GPIO to IMAGER connector pin input/output mapping. The default data is 0b00000000. This mapping is shown in the table below.

Table 12: Register 13, Imager Internal I/O Direction Register 1

Bit #	Function	Mapping
7	0 = GPIO_MD16 to DM365 pin	0 = Outputs 1 = DM365 pins are inputs
6	0 = GPIO_MD15 to DM365 pin	0 = Outputs 1 = DM365 pins are inputs
5	0 = GPIO_MD14 to DM365 pin	0 = Outputs 1 = DM365 pins are inputs
4	0 = GPIO_MD13 to DM365 pin	0 = Outputs 1 = DM365 pins are inputs
3	0 = GPIO_MD12 to DM365 pin	0 = Outputs 1 = DM365 pins are inputs
2	0 = GPIO_MD11 to DM365 pin	0 = Outputs 1 = DM365 pins are inputs
1	0 = GPIO_MD10 to DM365 pin	0 = Outputs 1 = DM365 pins are inputs
0	0 = GPIO_MD9 to DM365 pin	0 = Outputs 1 = DM365 pins are inputs

2.1.1.2.15 Register 14, Imager Internal I/O Mux Register 2

Register 14 is a 8 bit, read/write register that controls DM365 GPIO Muxing to IMAGER connector pin input. The default data is 0b00000000. The table below shows this muxing.

Table 13: Register 12, Imager Internal I/O Mux Register 2

Bit #	Muxing
7	0 = GPIO_MD12 MUX SELB
6	0 = GPIO_MD12 MUX SELA
5	0 = GPIO_MD11 MUX SELB
4	0 = GPIO_MD11 MUX SELA
3	0 = GPIO_MD10 MUX SELB
2	0 = GPIO_MD10 MUX SELA
1	0 = GPIO_MD9 MUX SELB
0	0 = GPIO_MD9 MUX SELA

2.1.1.2.16 Register 15, Imager Internal I/O Mux Register 3

Register 14 is a 8 bit, read/write register that controls DM365 GPIO Muxing to IMAGER connector pin input. The default data is 0b00000000. The table below shows this muxing.

Table 14: Register 15, Imager Internal I/O Mux Register 3

Bit #	Muxing
7	0 = GPIO_MD16 MUX SELB
6	0 = GPIO_MD16 MUX SELA
5	0 = GPIO_MD15 MUX SELB
4	0 = GPIO_MD15 MUX SELA
3	0 = GPIO_MD14 MUX SELB
2	0 = GPIO_MD14 MUX SELA
1	0 = GPIO_MD13 MUX SELB
0	0 = GPIO_MD13 MUX SELA

2.1.1.2.17 Register 16, Imager Internal I/O Direction Register 3

Register 16 is a 8 bit, read/write register that controls DM365 GPIO to IMAGER connector pin input/output mapping. The default data is 0b00000000. This mapping is shown in the table below.

Table 15: Register 16, Imager Internal I/O Direction Register 3

Bit #	Function	Mapping
7	Reserved	
6	0 = CCD_DDS_RST to DM365 pin	0 = Outputs 1 = DM365 pins are inputs
5	0 = PWM_CCD_SUB to DM365 pin	0 = Outputs 1 = DM365 pins are inputs
4	0 = GPIO_TACH to DM365 pin	0 = Outputs 1 = DM365 pins are inputs
3	0 = GPIO_MST_SLV to DM365 pin	0 = Outputs 1 = DM365 pins are inputs
2	0 = GPIO_MD19 to DM365 pin	0 = Outputs 1 = DM365 pins are inputs
1	0 = GPIO_MD18 to DM365 pin	0 = Outputs 1 = DM365 pins are inputs
0	0 = GPIO_MD17 to DM365 pin	0 = Outputs 1 = DM365 pins are inputs

2.1.1.2.18 Register 17, Imager Internal I/O Mux Register 4

Register 17 is a 8 bit, read/write register that controls DM365 GPIO Muxing to IMAGER connector pin input. The default data is 0b00000000. The table below shows this muxing.

Table 16: Register 17, Imager Internal I/O Mux Register 4

Bit #	Muxing
7	0 = GPIO__MST_SLV MUX SELB
6	0 = GPIO__MST_SLV MUX SELA
5	0 = GPIO_MD19 MUX SELB
4	0 = GPIO_MD19 MUX SELA
3	0 = GPIO_MD18 MUX SELB
2	0 = GPIO_MD18 MUX SELA
1	0 = GPIO_MD17 MUX SELB
0	0 = GPIO_MD17 MUX SELA

2.1.1.2.19 Register 18, Imager Internal I/O Mux Register 5

Register 18 is a 8 bit, read/write register that controls DM365 GPIO Muxing to IMAGER connector pin input. The default data is 0b00000000. The table below shows this muxing.

Table 17: Register 17, Imager Internal I/O Mux Register 5

Bit #	Muxing
7	Reserved
6	Reserved
5	0 = CCD_DDS_RST MUX SELB
4	0 = CCD_DDS_RST MUX SELA
3	0 = PWM_CCD_SUB MUX SELB
2	0 = PWM_CCD_SUB MUX SELA
1	0 = GPIO_TACH MUX SELB
0	0 = GPIO_TACH MUX SELA

2.1.1.2.20 Register 19, Board RESET Register

Register 19 is a 8 bit, read/write register that allows the user to select reset to major external peripherals. The default data is 0b00000000. The table below shows the mapping of these bits.

Table 18: Register 19, Board RESET Register

Bit #	RESET Signal	State Action
7	Reserved	N/A
6	Reserved	N/A
5	Reserved	N/A
4	Reserved	N/A
3	ETHERNET_RESET	1 = Force Reset to Logic 0 0 = Map Reset to CPLD inputs
2	TVP7002_RESET	1 = Force Reset to Logic 0 0 = Map Reset to CPLD inputs
1	IC3106_RESET	1 = Force Reset to Logic 0 0 = Map Reset to CPLD inputs
0	TVP5146_RESET	1 = Force Reset to Logic 0 0 = Map Reset to CPLD inputs

2.1.1.2.21 Register 720, CCD Internal I/O Direction Register 1

Register 720 is a 8 bit, read/write register that controls CPLD GPIO to CCD Connector pin input/output mapping. The default data is 0b11111111. The table below shows the mapping of these bits.

Table 19: Register 720, CCD Internal I/O Direction Register 1

Bit #	Signal	State Action
7	0 = GPIO_0.7DIR	0 = Outputs, 1 = Inputs
6	0 = GPIO_0.6DIR	0 = Outputs, 1 = Inputs
5	0 = GPIO_0.5DIR	0 = Outputs, 1 = Inputs
4	0 = GPIO_0.4DIR	0 = Outputs, 1 = Inputs
3	0 = GPIO_0.3DIR	0 = Outputs, 1 = Inputs
2	0 = GPIO_0.2DIR	0 = Outputs, 1 = Inputs
1	0 = GPIO_0.1DIR	0 = Outputs, 1 = Inputs
0	0 = GPIO_0.0DIR	0 = Outputs, 1 = Inputs

2.1.1.2.22 Register 721, CCD Internal I/O Read/Write Register 1

Register 721 is a 8 bit, read/write register that controls CPLD GPIO input on read, and out value on write. The default data is 0b00000000. The table below shows the mapping of these bits.

Table 20: Register 721, CCD Internal I/O Read/Write Register 1

Bit #	Signal	State Action
7	0 = GPIO_0.7	Write bit when DIR = 0 Read bit when DIR = 1
6	0 = GPIO_0.6	Write bit when DIR = 0 Read bit when DIR = 1
5	0 = GPIO_0.5	Write bit when DIR = 0 Read bit when DIR = 1
4	0 = GPIO_0.4	Write bit when DIR = 0 Read bit when DIR = 1
3	0 = GPIO_0.3	Write bit when DIR = 0 Read bit when DIR = 1
2	0 = GPIO_0.2	Write bit when DIR = 0 Read bit when DIR = 1
1	0 = GPIO_0.1	Write bit when DIR = 0 Read bit when DIR = 1
0	0 = GPIO_0.0	Write bit when DIR = 0 Read bit when DIR = 1

2.1.1.2.23 Register 722, CCD Internal I/O Direction Register 2

Register 722 is a 8 bit, read/write register that controls CPLD GPIO to CCD Connector pin input/output mapping. The default data is 0b11111111. The table below shows the mapping of these bits.

Table 21: Register 722, CCD Internal I/O Direction Register 2

Bit #	Signal	State Action
7	0 = GPIO_1.7DIR	0 = Outputs, 1 = Inputs
6	0 = GPIO_1.6DIR	0 = Outputs, 1 = Inputs
5	0 = GPIO_1.5DIR	0 = Outputs, 1 = Inputs
4	0 = GPIO_1.4DIR	0 = Outputs, 1 = Inputs
3	0 = GPIO_1.3DIR	0 = Outputs, 1 = Inputs
2	0 = GPIO_1.2DIR	0 = Outputs, 1 = Inputs
1	0 = GPIO_1.1DIR	0 = Outputs, 1 = Inputs
0	0 = GPIO_1.0DIR	0 = Outputs, 1 = Inputs

2.1.1.2.24 Register 723, CCD Internal I/O Read/Write Register 2

Register 723 is a 8 bit, read/write register that controls CPLD GPIO input on read, and out value on write. The default data is 0b00000000. The table below shows the mapping of these bits.

Table 22: Register 723, CCD Internal I/O Read/Write Register 2

Bit #	Signal	State Action
7	0 = GPIO_0.7	Write bit when DIR = 0 Read bit when DIR = 1
6	0 = GPIO_0.6	Write bit when DIR = 0 Read bit when DIR = 1
5	0 = GPIO_0.5	Write bit when DIR = 0 Read bit when DIR = 1
4	0 = GPIO_0.4	Write bit when DIR = 0 Read bit when DIR = 1
3	0 = GPIO_0.3	Write bit when DIR = 0 Read bit when DIR = 1
2	0 = GPIO_0.2	Write bit when DIR = 0 Read bit when DIR = 1
1	0 = GPIO_0.1	Write bit when DIR = 0 Read bit when DIR = 1
0	0 = GPIO_0.0	Write bit when DIR = 0 Read bit when DIR = 1

2.1.1.2.25 Register 724, CCD Internal I/O Direction Register 3

Register 724 is a 8 bit, read/write register that controls CPLD GPIO to CCD Connector pin input/output mapping. The default data is 0b11111111. The table below shows the mapping of these bits.

Table 23: Register 724, CCD Internal I/O Direction Register 3

Bit #	Signal	State Action
7	0 = GPIO_2.7DIR	0 = Outputs, 1 = Inputs
6	0 = GPIO_2.6DIR	0 = Outputs, 1 = Inputs
5	0 = GPIO_2.5DIR	0 = Outputs, 1 = Inputs
4	0 = GPIO_2.4DIR	0 = Outputs, 1 = Inputs
3	0 = GPIO_2.3DIR	0 = Outputs, 1 = Inputs
2	0 = GPIO_2.2DIR	0 = Outputs, 1 = Inputs
1	0 = GPIO_2.1DIR	0 = Outputs, 1 = Inputs
0	0 = GPIO_2.0DIR	0 = Outputs, 1 = Inputs

2.1.1.2.26 Register 725, CCD Internal I/O Read/Write Register 3

Register 725 is a 8 bit, read/write register that controls CPLD GPIO input on read, and out value on write. The default data is 0b00000000. The table below shows the mapping of these bits.

Table 24: Register 725, CCD Internal I/O Read/Write Register 1

Bit #	Signal	State Action
7	0 = GPIO_0.7	Write bit when DIR = 0 Read bit when DIR = 1
6	0 = GPIO_0.6	Write bit when DIR = 0 Read bit when DIR = 1
5	0 = GPIO_0.5	Write bit when DIR = 0 Read bit when DIR = 1
4	0 = GPIO_0.4	Write bit when DIR = 0 Read bit when DIR = 1
3	0 = GPIO_0.3	Write bit when DIR = 0 Read bit when DIR = 1
2	0 = GPIO_0.2	Write bit when DIR = 0 Read bit when DIR = 1
1	0 = GPIO_0.1	Write bit when DIR = 0 Read bit when DIR = 1
0	0 = GPIO_0.0	Write bit when DIR = 0 Read bit when DIR = 1

2.1.1.3 Key Pad Interface

The DM365 has an internal key pad controller. The key pad interface is multiplexed with the address lines on the asynchronous EMIF. CBTLV multiplexers are used to redirect the key pad interface to the key pad matrix. This interface can only be used when CE0 is in the NAND configuration. A control bit in the CPLD enables the Mux select on the CBTLV multiplexers. The 16 bit switch key pad matrix is set up on a 4 x 4 matrix on the EVM. The mapping of the switches are shown in the table below.

Table 25: Key Pad Layout

	Key-A0	**Key-A0**	**Key-A1**	**Key-A1**
Key-B0	SW6 / KEY 2	SW7 / LEFT	SW8 / EXIT	SW9 / DOWN
Key-B0	SW10 / ENTER	SW11 / UP	SW12 KEY 1	SW13 / RIGHT
Key-B1	SW14 / MENU	SW15 / REC	SW16 / REW	SW17 / SKIP-
Key-B1	SW18 / STOP	SW19 / FF	SW20 / SKIP+	SW2 / PLAY/ PAUSE

2.1.2 DDR2 Memory Interface

The DM365 device incorporates a dedicated 16 bit wide DDR2 memory bus. The EVM uses a single 1 gigabit 16 bit wide memory on this bus, for a total of 128 megabytes of memory for program, data, and video storage. The internal DDR controller uses a PLL to control the DDR memory timing. Memory refresh for DDR2 is handled automatically by the DM365 internal DDR controller.

2.1.3 Media Card Interface

The EVM supports 1 SD/MMC/MS and 1 SD/MMC media card interfaces. The MMC/SD0 port is dedicated to the SD/MMC/MS media card. The insert and write protect status can be read via CPLD register. MMC/SD1 port is configured to a second SD/MMC media card. This port is multiplexed via CBTLV switches to be used as general purpose I/O pins when the CPLD is appropriately configured for I/O multiplexing. The insert and write protect pin status can be read via a CPLD register.

2.1.4 UART Interface

The internal UART0 on the DM365 device is driven to connector P1. The UART's interface is routed to the RS-232 line drivers prior to being brought out to a DB-9 connector, P1.

2.1.5 USB Interface

The DM365 incorporates an on chip USB II controller. This interface is brought out to a mini A/B connector. Two jumpers are provided to make a flexible Host peripheral, and USB On The Go interface. J26 is used to manually select the ID pin state. J6 is used to add additional capacitance to VBUS for host mode operation. A TPS2065 is used to power VBUS via DRV_VBUS signal for Host mode applications. The CPLD selects the source pin for DRV_VBUS signals via internal CPLD registers.

2.2 Input Video Port Interfaces/Imager Input Ports

The DM365 EVM supports composite, component, or imager video capture. CBT multiplexers selected via CPLD registers chose the interface that is connected to the DM365 video input port. A Texas Instruments TVP5146 is used to decode composite video or S-video inputs into the device. J15 is used for the S-video inputs and J13 for the composite inputs on the EVM.

A TVP7002 provides component image capture up to 720P resolution.

J11, J8, J9 interface to a THS7353 amplifier/filter which interfaces directly to the TVP7002 which drives the DM365 input port.

J10, a DIN96 connector allows users to support imager interfaces. This is mapped directly to the video input port via CBT mux. The figure below shows this mapping,

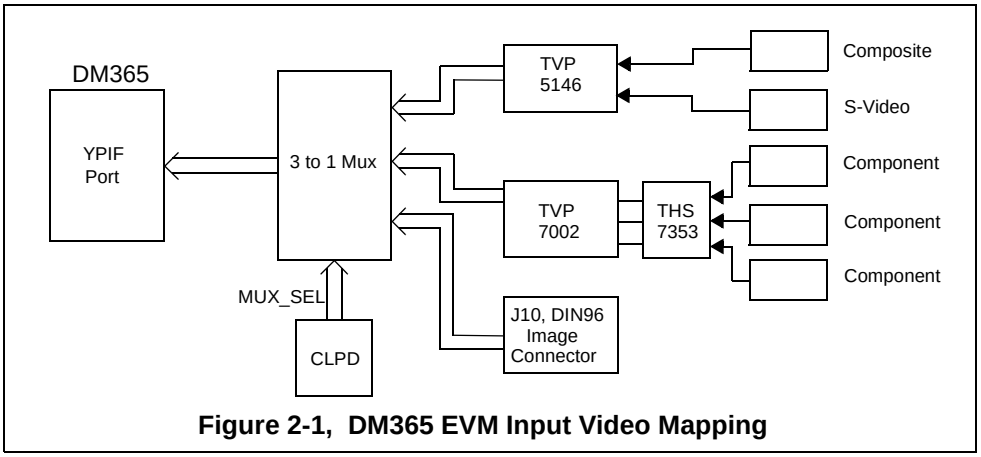


Figure 2-1, DM365 EVM Input Video Mapping

2.2.1 On Chip Video Output DAC

The DM365 incorporates 1 TV composite video output DAC and 3 component video DACs to interface to composite and component video outputs. The TV Out DAC is filtered and driven to RCA jack, J16.

The component output DACs are driven into a THS7303 video amplifier and output to RCA connectors J21, J17, J20.

2.2.2 LCD Video Connectors

The DM365 incorporates 3 interface connectors; J18, J19, and J23 for digital video output for interfacing to LCD displays. The pinouts for these displays are detailed in section 3 of this manual.

2.3 AIC3101 Interface

The EVM uses a Texas Instruments TLV320AIC3101 stereo codec for input and output of audio signals. The codec samples analog signals on the microphone or line inputs and converts them into digital data so it can be processed by the DSP. When the DSP is finished with the data it uses the codec to convert the samples back into analog signals on the line output so the user can hear the output.

The codec communicates using two serial channels, one to control the codec's internal configuration registers and one to send and receive digital audio samples. The I^2C bus is used as the AIC3101's control channel. The control channel is generally only used when configuring the codec, it is typically idle when audio data is being transmitted,

The DM365's McBSP is used as the bi-directional data channel. All audio data flows through the data channel. Many data formats are supported based on the three variables of sample width, clock signal source and serial data format. The EVM examples generally use a 16-bit sample width with the codec in master mode so it generates the frame sync and bit clocks at the correct sample rate without effort on the DSP side.

The codec is clocked via a 27 Mhz oscillator. The internal sample rate generator subdivides the default system clock to generate common audio frequencies. The sample rate is set by a codec register. The figure below shows the codec interface on the DM365 EVM.

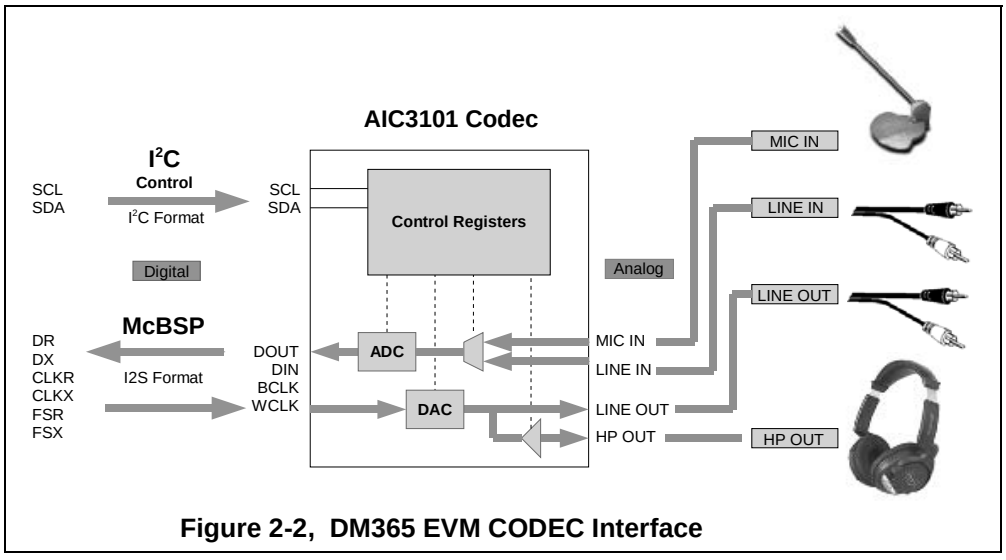


Figure 2-2, DM365 EVM CODEC Interface

2.4 On Chip Voice Codec

The DM365 integrates a single channel voice codec. The input for this codec is connected to on board microphone M1. The output of this codec is connected to on board speaker SPK1.

2.5 On Chip Analog to Digital Converter (ADC)

The DM365 has an on chip 6 channel Analog to Digital Converter (ADC). Four of the channels are interfaced to on board voltages and two channels are connected to test points as shown in the table below.

Table 26: On Chip Analog to Digital Converter

Channel	Input Signal
ADC_CH0	CCD_PSMON
ADC_CH1	VCC_3V3
ADC_CH2	CPU_VCC_1V8
ADC_CH3	VCC_1V2
ADC_CH4	TP37
ADC_CH5	TP36

2.6 On Chip RTC

The DM365 integrates an on chip real time clock. The Real Time Clock is battery backed up via TPS65510 and Battery BHT1. The EVM is not shipped with a backup battery. The mode of operation for the Real Time Clock is configured via switch SW23, as defined in section 3.

2.7 Ethernet Interface

The DM365 incorporates an internal MII ethernet MAC which interfaces to a Mircel 10/100 ethernet Phy. The 10/100 Mbit interface is isolated and brought out to a RJ-45 standard ethernet connector, P2. The ethernet address is stored in the on board I^2C EEPROM manufacturing.

For GPIO modes of operation when the MII interface is not used CBTLV multiplexes and directs the I/O to the on board CPLD used as imager expansion I/Os.

The RJ-45 has 2 LEDs integrated into its connector. The LEDs are green and yellow and indicate the status of the ethernet link. The green LED, when on, indicates link and when blinking indicates link activity. The yellow LED, when illuminated, indicates full duplex mode.

2.8 I^2C Interface

The I^2C bus on the DM365 is ideal for interfacing to the control registers of many devices. On the DM365 EVM the I^2C bus is used to configure the video decoders, stereo Codec, video amplifiers, I2C EEPROM, and communicate with the MSP430. An I^2C ROM is also interfaced via the serial bus. The format of the bus is shown in the figure below.

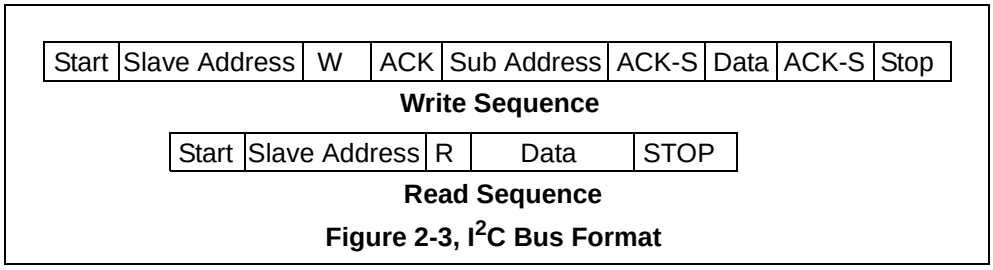


Figure 2-3, I^2C Bus Format

The addresses of the on board peripherals are shown in the table below.

Table 27: I^2C Memory Map

Device	Address	R/W	Function
AIC3101	0x18	R/W	CODEC
MSP430	0x25	R/W	IR Controller
THS7303	0x2C	R/W	Video Output Amplifier
THS7353	0x2E	R/W	Video Input Amplifier
CAT24C256	0x50	R/W	I^2C EEROM
TVP7002	0x5C	R/W	Component Decoder
TVP5146	0x5D	R/W	Composite 1 Decoder

2.8.1 MSP430

The DM365 EVM incorporates infrared remote, interface using a MSP430 microcontroller. The I^2C interface is used on the DM365 processor to communicate to the MSP430. The MSP430 acts as a slave device on the I^2C bus.

2.9 Daughter Card Interfaces

The EVM provides expansion connectors that can be used to accept plug-in daughter cards. The daughter card allows users to build on their EVM platform to extend its capabilities and provide customer and application specific interfaces. The Asynchronous EMIF is brought out to J14. The video digital output port is brought out to the daughter card interface along with I/O and imager interface is brought out to a DIN96 connector as detailed previously.

2.10 DM365 CPU/Video Clocks

The DM365 EVM uses a 24 Megahertz crystal to generate the main input clock. The DM365 has multiple internal PLLs which can multiply the input clock to generate the internal clocks. The PLL's multipliers are set via software on the DM365 device.

The Real Time clock uses a 32,768 hertz crystal.

2.11 Battery

The DM365 EVM incorporates a battery holder to provide backup power to the internal real time clock when the power is not applied to the board. The optional battery should be +3 volt 20 millimeter coin type Lithium single cell.

Some common part numbers for batteries which should operate in the EVM are shown in the table below.

Table 28: Battery Part Numbers

Part Numbers
CR2032
DL2032
BR2032
CR2025
BR2025
CR2016
BR2016
DL2016

These batteries are available from Duracell, Eveready, Panasonic, Ray-O-Vac, Sanyo, Sony, Sieko, Toshiba, Varta, and other battery manufacturers.

Chapter 3

Physical Description

This chapter describes the physical layout of the DM365 EVM and its interfaces.

Topic **Page**

Topic		Page

3.1 Board Layout

The DM365 EVM is a 8.0 x 8.7 inch (203 x 221 mm.) ten (10) layer printed circuit board which is powered by an external +5 volt only power supply. Figure 3-1 shows the layout of the top side of the DM365 EVM.

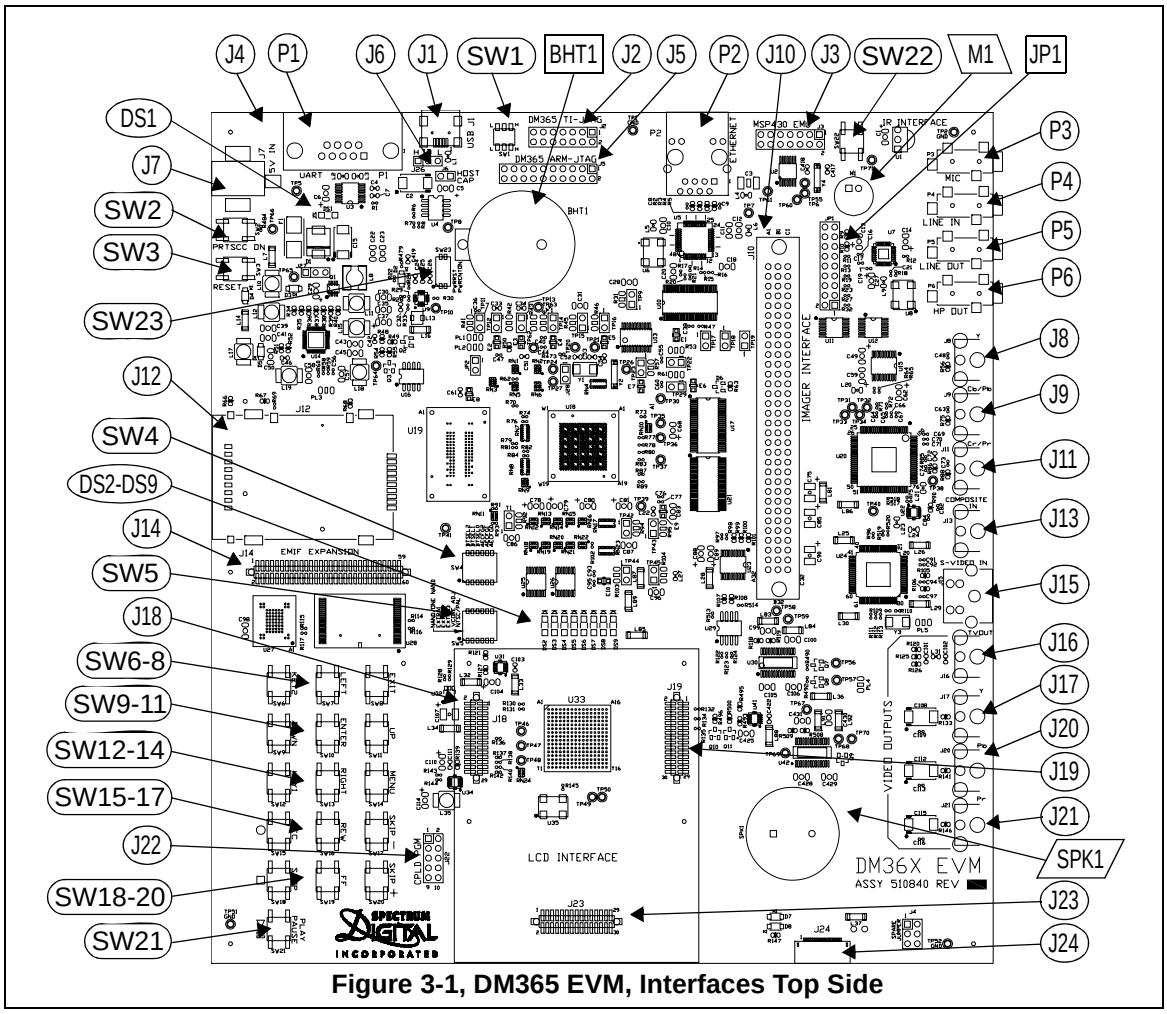


Figure 3-1, DM365 EVM, Interfaces Top Side

Figure 3-2 shows the layout of the bottom side of the DM365 EVM.

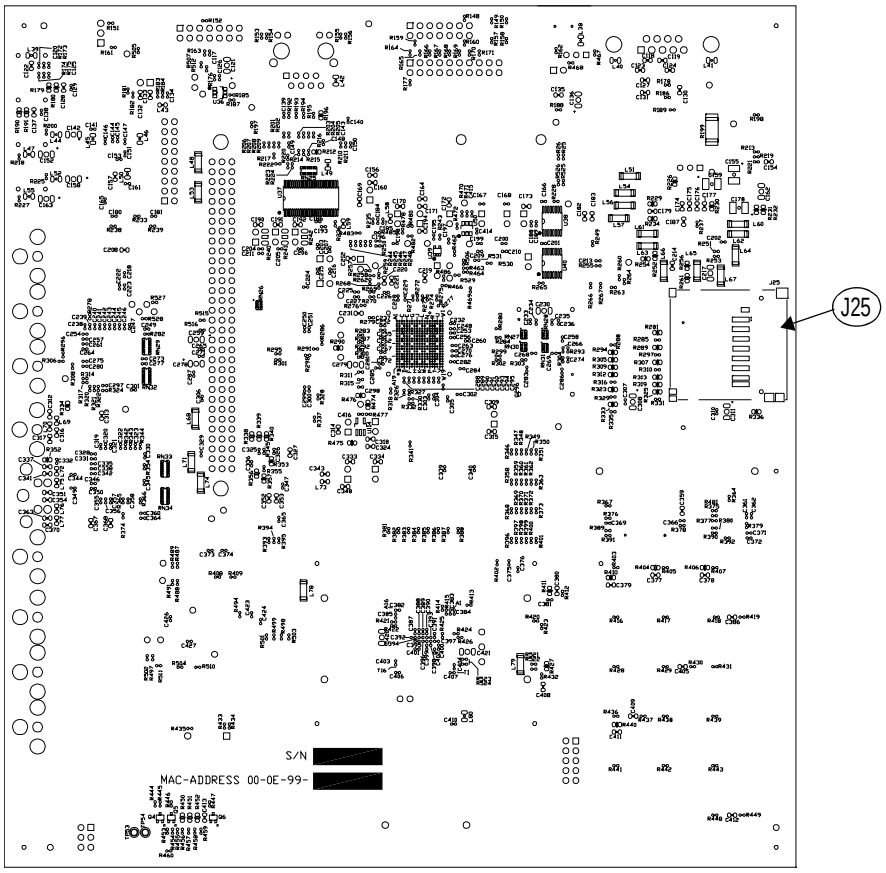


Figure 3-2, DM365 EVM, Interfaces Bottom Side

3.2 Connectors

The DM365 EVM has numerous connectors, option jumpers, and interfaces to control and provide connections to various peripherals. These connectors and jumpers are described in the following sections.

Table 1: DM365 Connectors

Connector	Size	Function
J1	1 x 4	USB MiniAB Connector
J2	2 x 7	14 Pin TI JTAG Emulation Header
J3	7 x 2	MSP430 JTAG Header
J4	3 x 2	Spare Jumper Holder
J5	10 x 2	20 Pin ARM JTAG Emulation Header
J6	2 x 1	USB Capacitor Select
J7	2	+5 Volts In
J8	2	Y Component Video In, RCA Jack (Grn)
J9	2	Pb Component Video In, RCA Jack (Blue)
J10	32 x 3	Imager Interface
J11	2	Pr Component Video In, RCA Jack (Red)
J12	2	SD/MMC/MS Card Interface
J13	2	CVBS/Y Input, RCA Jack (Yellow)
J14	30 x 2	EMIF/UPHI DC Interface
J15	4	S-video In, DIN connector
J16	2	Composite TV Out, RCA Jack (Yellow)
J17	2	Y Component Video Output, RCA Jack (Green)
J18	15 x 2	Video Output DC
J19	15 x 2	Video Output DC
J20	2	Pb Component Video Output, RCA Jack (Blue)
J21	2	Pr Component Video Output, RCA Jack (Red)
J22	5 x 2	CPLD Programming Header
J23	15 x 2	I/O Interface Header
J24	20 x 1	DILC Host Connector
J25	9	MMC/SD Card Interface
P1	9	RS-232 UART
P2	6	Ethernet Interface
P3	4	Microphone In
P4	4	Line In
P5	4	Line Out
P6	4	Headphone Out
U1	3	Infrared Interface
SPK1	2	Speaker
BHT1	2	Battery Holder
M1	2	Microphone

3.2.1 J1, USB MiniAB Connector and Jumpers

Connector J1 is a mini A/B USB connector. The pinout for the J1 connector is shown in the table below.

Table 2: J1, MiniAB USB Connector

Pins	Signal
1	USB_VBUS_CONN
2	USB_DM
3	USB_DP
4	USB_ID
5	GND

The EVM incorporates the ability to toggle the ID pin on the USB connector via software control. The USB_ID pin on the DM365 controls this function.

For “USB ON The Go” mode remove jumper J6. This will allow the cable to configure the ID pin on the DM365 processor.

The EVM supplies up to 500 ma of current to the USB_VBUS via a TPS61092 DC/DC converter. This is enabled via the DM365’s DRV_VBUS pin. J50 supplies extra capacitance for host mode operations. Remove J50 for “USB On The Go” operations. Spare jumpers can be stored on connector J4.

3.2.2 J2, 14 Pin External JTAG Connector

Connector J2 is a 2 x 7 double row male header with pin 6 clipped to serve as a key. This is the standard interface used by JTAG emulators to interface to Texas Instruments processors. The pinout for the connector is shown in the figure below.

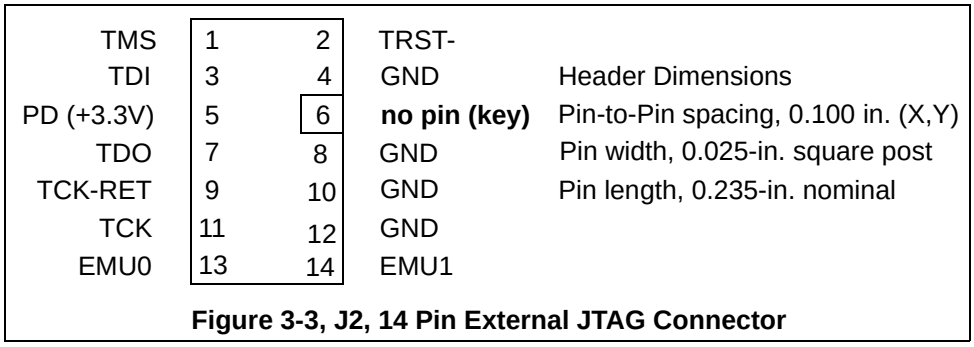


Figure 3-3, J2, 14 Pin External JTAG Connector

The signal names for each pin are shown in the table below.

Table 3: J2, 14 Pin External JTAG Connector

Pin #	Signal Name	Pin #	Signal Name
1	TMS	2	TRST-
3	TDI	4	GND
5	PD	6	no pin - key
7	TDO	8	GND
9	TCKRET	10	GND
11	TCK	12	GND
13	EMU0	14	EMU1

* **Note:** EMU0/EMU1 mode must be selected to ICEPICK mode

3.2.3 J3, MSP430 JTAG Header

The J3, MSP430 JTAG header, is located on the top side of the board and is used to provide a programming interface to the MSP430 microcontroller. The pinout for the J3 connector is shown in the table below. This connector is typically used for factory use only.

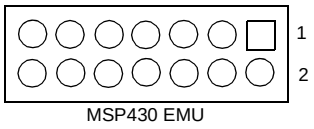


Figure 3-4, J3, MSP430 JTAG Header

Table 4: J3, MSP430 JTAG Header

Pin #	Signal	Pin #	Signal
1	430_TDO/TDI	2	NC
3	NC	4	MSP430_3V3
5	NC	6	NC
7	TCK	8	NC
9	GND	10	NC
11	NC	12	NC
13	NC	14	NC

3.2.4 J4, Spare Jumper Holder

J4 is a 3 x 2 connector used to hold unused jumper plugs that from time to time may be required in other connectors/jumpers on the D365 EVM. The pins on this connector are not connected to any signals.

3.2.5 J5, 20 Pin ARM JTAG Emulation Header

The J5 emulation header is located on the top side of the board and is used to provide an interface to ARM compatible JTAG emulators. The pinout for this connector is shown in the table below.

Table 5: J5, 20 Pin ARM JTAG Emulation Header

Pin #	Signal	Pin #	Signal
1	VCC_3V3	2	VCC_3V3
3	ARM_TRSTn	4	Ground
5	ARM_TDI	6	Ground
7	ARM_TMS	8	Ground
9	ARM_TCK	10	Ground
11	ARM_TCKRET	12	Ground
13	ARM_TDO	14	Ground
15	ARM_RSTn	16	Ground
17	NC	18	Ground
19	NC	20	Ground

* **Note:** EMU0/EMU1 switch must be set to ARM mode

3.2.6 J6, USB Capacitance Select

The J6 jumper is used to provide more capacitance when the USB connector is used in the host mode. When the jumper is shorted the extra capacitance is provided. These open and shorted position are shown below.

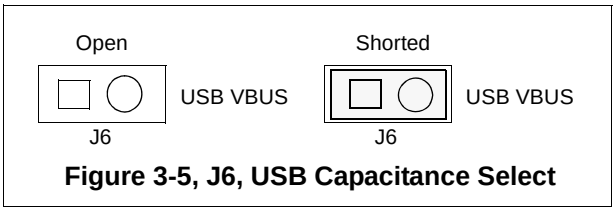


Figure 3-5, J6, USB Capacitance Select

Table 6: J6, USB Capacitance Select

Position	Function
Open	6.8 uF Capacitance
Shorted	106.8 uF Capacitance

3.2.7 J7, +5 Volts Input

Connector J7 is the input power connector. This connector brings in +5 volts to the EVM. This is a 2.5mm. jack. The inside of the jack is tied to through a fuse to VCC_5V. The other side is tied to ground and LED DS1. The figure below shows this connector as viewed from the card edge.

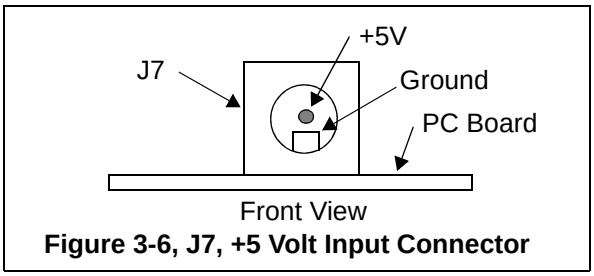


Figure 3-6, J7, +5 Volt Input Connector

3.2.8 J12, SD/MMC/MS Card Interface

The J12 SD/MMC/MS Card Interface connector is located on the top side of the board and is used to provide an interface to a SD/MMC/MS card. The pinout for the J12 connector is shown in the table below.

Table 7: J12, SD/MMC/MS Connector

Pin #	Signal	Pin #	Signal
1	SD.DATA3	2	SD.CMD
3	SD.VSS1	4	VCC_3V3
5	SD.CLK	6	SD.VSS2
7	SD.DATA0	8	SD.DATA1
9	SD.DATA2	10	GND
11	MS.BS	12	MS.DATA1
13	MS.SDIO/DATA0	14	MS.DATA2
15	MS.XINS	16	MS.DATA3
17	MS.CLK	18	VCC_3V3
19	GND	20	WP
21	INS	22	GND
23	GND		

3.2.9 J10, Imager Interface

Connector J10 is 32 x 3 connector used to interface to external imager logic. The pin out for this connector is shown in the table below.

Table 8: J10, Imager Interface

Pin	Signal	Pin	Signal	Pin	Signal
A1	Ground	B1	GPIO_MD10	C1	GND_STB
A2	Ground	B2	GPIO_MD9	C2	GND_STB
A2	CCD_PSMON	B2	GPIO_MD8	C2	3V3_STB
A4	GPIO_MD1	B4	GPIO_MD7	C4	5V_DC_J6
A5	5V_DC_J6	B5	5V_DC_J6	C5	5V_DC_J6
A6	GND_MTR	B6	MOT_PWR	C6	GPIO_MD19
A7	GND_MTR	B7	MOT_PWR	C7	GPIO_MD18
A8	NC	B8	CCD_DATA0	C8	GPIO_MST_SLV
A9	CDD_DATA2	B9	CCD_DATA15	C9	GPIO_MD17
A10	Ground	B10	CCD_DATA1	C10	GPIO_MD16
A11	CDD_DATA3	B11	GPIO_MD6	C11	GPIO_MD15
A12	Ground	B12	GPIO_MD5	C12	GPIO_MD14
A13	CDD_DATA4	B13	GPIO_MD4	C13	GPIO_MD13
A14	Ground	B14	Ground	C14	GPIO_TACH
A15	CDD_DATA5	B15	PWM_CCD_SUB	C15	GPIO_MD12
A16	Ground	B16	CCD_DDSRST	C16	GPIO_MD11
A17	CDD_DATA6	B17	GPIO_MD3	C17	I2C_DATA
A18	Ground	B18	GPIO_MD2	C18	I2C_SCLK
A19	CDD_DATA7	B19	SPI4_SDO	C19	VCC_CCD15V
A20	Ground	B20	SPI4_SCLK	C20	VCC_CCD15V
A21	CDD_DATA8	B21	Ground	C21	VCC_CCD_N75V
A22	Ground	B22	CDD_PCLK	C22	VCC_CCD_N75V
A23	CDD_DATA9	B23	Ground	C23	3V3_CCD
A24	Ground	B24	CDD_WEN	C24	3V3_CCD
A25	CDD_DATA10	B25	Ground	C25	5V_DC_J6
A26	Ground	B26	CDD_FIELD	C26	5V_DC_J6
A27	CDD_DATA11	B27	Ground	C27	Ground
A28	Ground	B28	CDD_HSYNC	C28	Ground
A29	CDD_DATA12	B29	Ground	C29	3V3A_CCD
A30	Ground	B30	CDD_VSYNC	C30	3V3A_CCD
A31	CDD_DATA13	B31	Ground	C31	AGND_IMAGER
A32	Ground	B32	CDD_DATA14	C32	AGND_IMAGER

3.2.10 J14, EMIF/UPI DC Interface

Table 9: J14, EMIF/UPI DC Interface

Pin	Signal	Pin	Signal
2	Ground	1	Ground
4	EM_D0	3	EM_D1
6	EM_D2	5	EM_D3
8	EM_D4	7	EM_D5
10	EM_D6	9	EM_D7
12	Ground	11	Ground
14	EM_D8	13	EM_D9
16	EM_D10	15	EM_D11
18	EM_D12	17	EM_D13
20	EM_D14	19	EM_D15
22	Ground	21	Ground
24	EM_WAIT	23	EM_CLK
26	Ground	25	Ground
28	EM_CE0	27	EM_ADV
30	Ground	29	Ground
32	EM_CE1	31	EM_WE
34	Ground	33	Ground
36	EMIF_SEL	35	EM_OE
38	Ground	37	Ground
40	EM_BA0	39	EM_BA1
42	EM_A0	41	EM_A1
44	EM_A2	43	EM_A3
46	EM_A4	45	EM_A5
48	Ground	47	Ground
50	EM_A6	49	EM_A7
52	EM_A8	51	EM_A9
54	EM_A10	53	EM_A11
56	EM_A12	55	EM_A13
58	VCC_3V3	57	VCC_3V3
60	VCC_5V	59	VCC_5V

3.2.11 J8, Y Component Video In, RCA Jack (Green)

J8 is an RCA jack used as a Y component input to the THS7353, U15, pin 3. The figure below shows this connector as viewed from the card edge.

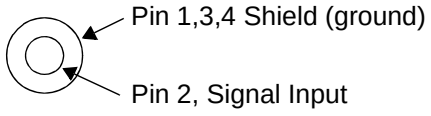


Figure 3-7, J8, Y Component Video In, RCA Jack

Table 10: J8, Y Component Video In, RCA Jack

Pin #	Signal Name
1	TVP_AGND
2	CH2-INA, U15, Pin 3
3	TVP_AGND
4	TVP_AGND

3.2.12 J9, Pb Component Video In, RCA Jack (Blue)

J9 is an RCA jack used as a Pb component input to the THS7353, U15, pin 4. The figure below shows this connector as viewed from the card edge.

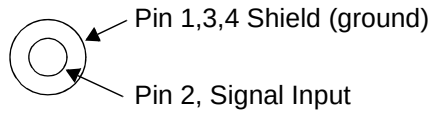


Figure 3-8, J9, Pb Component Video In, RCA Jack

Table 11: J9, Pb Component Video In, RCA Jack

Pin #	Signal Name
1	TVP_AGND
2	CH3-INA, U15, Pin 4
3	TVP_AGND
4	TVP_AGND

3.2.13 J11, Pr Component Video In, RCA Jack (Red)

J11 is an RCA jack used as a Pr component input to the THS7353, U15, pin 2. The figure below shows this connector as viewed from the card edge.

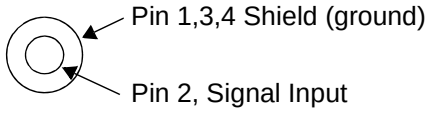


Figure 3-9, J11, Pr Component Video In, RCA Jack

Table 12: J11, Pr Component Video In, RCA Jack

Pin #	Signal Name
1	TVP_AGND
2	CH1-INA, U15, Pin 2
3	TVP_AGND
4	TVP_AGND

3.2.14 J15, S-Video In

Connector J15 is a four pin mini din connector which interfaces to the TVP5146 encoder, U24. This connector brings in a video signal (LUMA) to pin 9 on the TVP5146. Do **NOT** plug into this connector with the power on. The figure below shows this connector as viewed from the card edge.

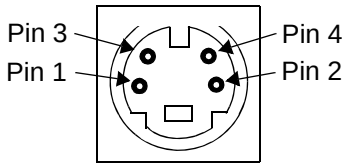


Figure 3-10, J15, Front View, Mini Din Connector

Table 13: J15, S-Video In, Mini Din Connector

Pin #	Signal Name
1	GND
2	GND
3	VI_1_C, U24, Pin 2
4	Chroma

3.2.15 J13, CVBS/Y Input, RCA Jack (Yellow)

J13 is an RCA jack used as the CVBS/Y input to the TVP5146. The figure below shows this connector as viewed from the card edge.

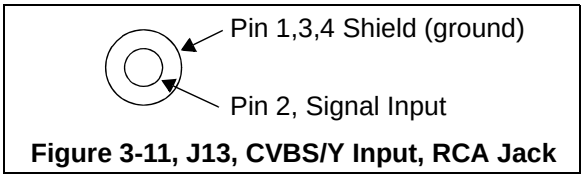


Figure 3-11, J13, CVBS/Y Input, RCA Jack

Table 14: J13, CVBS/Y Input, RCA Jack

Pin #	Signal Name
1	DEC_GND
2	VI_2_B, U24, Pin 8, TVP5146
3	DEC_GND
2	DEC_GND

3.2.16 J16, Composite TV Out, RCA Jack (Yellow)

J16 is an RCA jack used as a TV output from the DM365. This connector brings out a TV signal. The figure below shows this connector as viewed from the card edge.

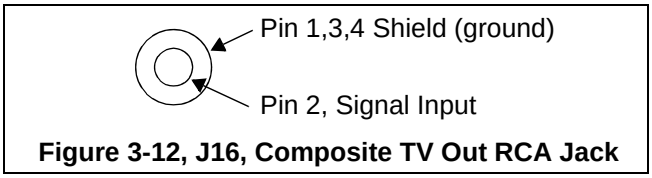


Figure 3-12, J16, Composite TV Out RCA Jack

Table 15: J16, Composite TV Out, RCA Jack

Pin #	Signal Name
1	DEC_GND
2	U18-3, Pin A10
3	DEC_GND
2	DEC_GND

3.2.17 J17, Y Component Video Out, RCA Jack (Green)

J17 is an RCA jack used as a green component output from the THS7303 DAC, U23, pin 17, signal CH2-OUT. The figure below shows this connector as viewed from the card edge.

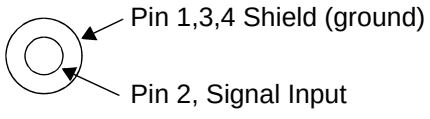


Figure 3-13, J17, Y Component Video Out, RCA Jack

Table 16: J17, Y Component Video Out, RCA Jack

Pin #	Signal Name
1	DENC_GND
2	THS7303 DAC, U23, pin 19,signal CH2-OUT
3	DENC_GND
4	DENC_GND

3.2.18 J20, Pb Component Video Out, RCA Jack (Blue)

J20 is an RCA jack used as a Pb component output from the THS7303 DAC, U23, pin 15, signal CH3-OUT. The figure below shows this connector as viewed from the card edge.

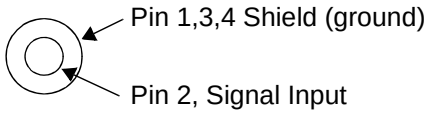


Figure 3-14, J20, Pb Component Video Out, RCA Jack

Table 17: J20, Pb Component Video Out, RCA Jack

Pin #	Signal Name
1	DENC_GND
2	THS7303 DAC, U23, pin 15,signal CH3-OUT
3	DENC_GND
2	DENC_GND

3.2.19 J21, Pr Component Video Output, RCA Jack (Red)

J21 is an RCA jack used as a Pr component output from the THS7303 DAC, U23, pin 19, signal CH1-OUT. The figure below shows this connector as viewed from the card edge.

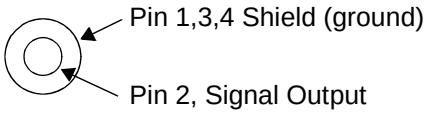


Figure 3-15, J21, Pr Component Video Out, RCA Jack

Table 18: J21, Pr Component Video Out, RCA Jack

Pin #	Signal Name
1	DENC_GND
2	THS7303 DAC, U23, pin 19, signal CH1-OUT
3	DENC_GND
4	DENC_GND

3.2.20 J18, J19, Video Output DC

Connectors J18 and J19 make up the interface to the video output DC interface. The signals on each of these connectors are shown in the tables below.

Table 19: J18, Video Output DC

Pin	Signal	Pin	Signal
1	BL_6V6	2	LCD_3V3
3	BL_6V6_RTN	4	LCD_3V3
5	Ground	6	Ground
7	VDOUT_VSYNC	8	NC
9	Ground	10	LCD_V5
11	VDOUT_HSYNC	12	LCD_V5
13	Ground	14	Ground
15	VDOUT_VCLK	16	CDOUT_FIELD
17	Ground	18	15V_LCD
19	BAT_VIN	20	15V_LCD
21	BAT_VIN	22	Ground
23	SPI1_SDI	24	VDOUT_EXTCLK
25	SPI1_SDENA0	26	I2C_DATA
27	SPI1_SDO	28	I2C_SCLK
29	SPI__SCLK	30	Ground

Table 20: J19, Video Output DC

Pin	Signal	Pin	Signal
1	VDOUT_Y0	2	VDOUT_C0
3	R1_GIO33	4	Ground
5	VDOUT_Y1	6	VDOUT_C1
7	R1_GIO32	8	Ground
9	VDOUT_Y2	10	VDOUT_C2
11	R1_GIO30	12	Ground
13	VDOUT_Y3	14	VDOUT_C3
15	Ground	16	Ground
17	VDOUT_Y4	18	VDOUT_C4
19	Ground	20	Ground
21	VDOUT_Y5	22	VDOUT_C5
23	Ground	24	Ground
25	VDOUT_Y6	26	VDOUT_C6
27	Ground	28	Ground
29	VDOUT_Y7	30	VDOUT_C7

3.2.21 J22, CPLD Programming Header

The J22, CPLD programming header, is for use by the factory. This header is not intended to be used outside the factory. The signals on this header are shown in the table below.

Table 21: J22, CPLD Programming Header

Pins	Signal	Pins	Signal
1	ISR_TCK	2	Ground
3	ISR_TDO	4	VCC_3V3
5	ISR_TMS	6	NC
7	NC	8	NC
9	ISR_TDI	10	Ground

3.2.22 J23, I/O Interface Header

Connector J23 is an I/O interface header allowing the user to connect external logic to interface with the I/O pins on the CPLD U33. The signals on this header are shown in the table below.

Table 22: J23, I/O Interface Header

Pins	Signal	Pins	Signal
2	VCC_1V8	1	VCC_1V8
4	NC	3	NC
6	CPLD.COMM_GIO6	5	CPLD.COMM_GIO7
8	CPLD.COMM_GIO16	7	CPLD.COMM_GIO17
10	CPLD.COMM_GIO54	9	CPLD.COMM_GIO67
12	CPLD.COMM_GIO65	11	CPLD.COMM_GIO31
14	CPLD.COMM_GIO63	13	CPLD.COMM_GIO64
16	CPLD.COMM_GIO62	15	CPLD.COMM_GIO61
18	CPLD.COMM_GIO60	17	CPLD.COMM_GIO59
20	CPLD.COMM_GIO58	19	CPLD.COMM_GIO57
22	CPLD.COMM_GIO56	21	CPLD.COMM_GIO32
24	NC	23	NC
26	NC	25	NC
28	CPLD.CONN_RESETn	27	NC
30	Ground	29	Ground

3.2.23 J24, DILC Host Connector

J24 is the DILC Host Connector. The signals on this connector are shown in the table below.

Table 23: J24, DILC Host Connector

Pins	Signal
1	CAM_PWR
2	CAM_PWR
3	SPI2_SCLK_DILC
4	Ground
5	SPI2_SDO_DILC
6	Ground
7	SPI2_SDI_DILC
8	Ground
9	LINEOUT
10	AVJ_DET
11	TP53
12	TP33
13	GIO_DILC_CHG_CTL
14	CD1
15	CD2
16	VBUS1
17	TP54
18	Ground
19	TVOUT
20	Ground
MP1	Ground
MP2	Ground

3.2.24 J25, MMC/SD Connector

The J25 MMC/SD connector is located on the bottom side of the board and is used to provide an interface to a MMC/SD card. The pinout for the J25 connector is shown in the table below.

Table 24: J25, MMC/SD Connector

Pin #	Signal	Pin #	Signal
1	CONN_SD1_DATA3	2	CONNSD1_CMD
3	GND	4	VCC_3V3
5	CONN_SD1_CLK	6	GND
7	CONN_SD1_DATA0	8	CONN_SD1_DATA1
9	CONN_SD1_DATA2	10	WP, VCC_3V3
11	GND	12	CARD_DETECT

3.2.25 P1, RS-232 UART

The P1 connector is a 9 pin male D-connector which provides a UART interface to the EVM. This connector interfaces to the MAX 3221 RS-232 line driver (U3) and is located on the top side of the board. A view of the connector from the card edge is shown in the figure below. The signals present on this connector are defined in the following table.

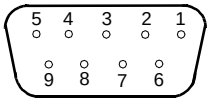


Figure 3-16, P1, DB9 Male Connector

The pin numbers and their corresponding signals are shown in the table below. This corresponds to a standard dual row to DB-9 connector interface used on personal computers.

Table 25: P1, RS-232 UART Pinout

Pin #	Signal Name
1	NC
2	R_IN, U3, Pin 8
3	T_OUT, U3, pin 13
4	NC
5	GND
6	NC
7	Pin 8
8	Pin 7
9	NC

3.2.26 P2, Ethernet Interface

The P2 connector is located on the top side of the board and is used to provide an Ethernet interface. P2 integrates the magnetics and standard RJ-45 connector. The two tables below show the signals present on the magnetics interface and the connector side.

Table 26: P2, Magnetics/LEDs Interface Signals

Pin #	Signal	Pin #	Signal
1	TX+, U5, Pin 41	2	TX-, U5, Pin 40
3	RX+, U5, Pin 33	4	VDD_3V3A
5	VDD_3V3A	6	RX-, U5, Pin 32
7	NC	8	GND_E_NET
9	VCC_3V3A	10	EPHY_LED2
11	VCC_3V3A	12	EPHY_LED0

The ethernet connector incorporates 2 LEDs which give link and transmit status from the ethernet controller.

Table 27: P2, RJ-45 Connector

Pin #	Signal	Pin #	Signal
1	TXD+	2	TXD-
3	RXD+	4	TXD-CT
5	RXD-CT	6	RXD-
7	NC	8	GND
9	LED1+	10	LED1-
11	LED2+	12	LED2-

3.2.27 P3, Microphone In

The microphone input, P3, is a 3.5 mm. stereo jack. Both inputs are connected to the microphone so it is monaural. The signal is connected to signals “MIC2R” and “MIC2L” of the TVL320AIC3101. The signals on the plug are shown in the figure below.

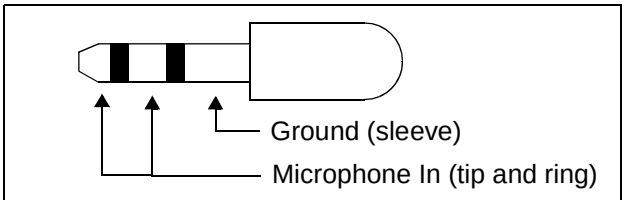


Figure 3-17, P3, Microphone Input Jack

Table 28: P3, Microphone Input Jack

Pin #	Signal Name
1	GND_AIC
2	MIC2L, MIC2R, U7, Pins 14,16
3	MIC2L, MIC2R, U7, Pins 14,16
4	GND_AIC

3.2.28 P4, Line In

Connector P4 is an audio stereo line input to the TVL320AIC3101, U7, on the EVM. The input connector is a 3.5 mm stereo jack. The signals on the mating plug are shown in the figure below.

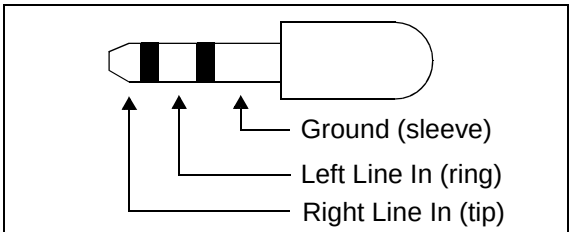


Figure 3-18, P4, Audio Stereo Line In Jack

Table 29: P4, Audio Stereo Line In

Pin #	AIC3101 Signal
1	GND_AIC
2	LINE1LP, U7, Pin 10
3	LINE1RP, U7, Pin 12
4	GND_AIC

3.2.29 P5, Line Out

The connector P5, is an audio stereo output from the TVL320AIC3101, U7, on the EVM. The output connector is a 3.5 mm stereo jack. The signals on the mating plug are shown in the figure below.

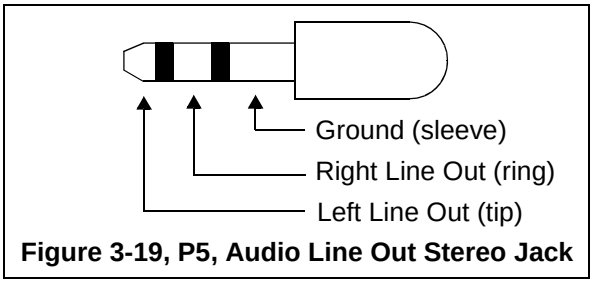


Figure 3-19, P5, Audio Line Out Stereo Jack

Table 30: P5, Audio Line Out Stereo Jack

Pin #	AIC3101 Signal
1	GND_AIC
2	LEFT_LO+, U7, Pin 27
3	RIGHT_LO+, U7, Pin 29
4	NC

3.2.30 P6, Headphone Out

The P6 connector is a 3.5 mm. stereo headphone output from the TVL320AIC3101, U7, on the EVM. This connector is located on the top side of the board. A view of the connector from the card edge is shown in the figure below. The signals present on this connector are defined in the following table.

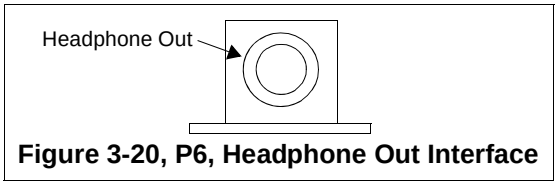


Figure 3-20, P6, Headphone Out Interface

Table 31: P6, Headphone Out Interface

Pin #	AIC3101 Signal
1	GND_AIC
2	HPLOUT, U7, Pin 19
3	HPROUT, U7, Pin 23
4	NC

3.2.31 U1, Infrared Interface

U1 is an infrared receiver mounted on the edge of the board. This device interfaces to the MSP430 mircrocontroller. The view of U1 is shown from a board edge view in the figure below.

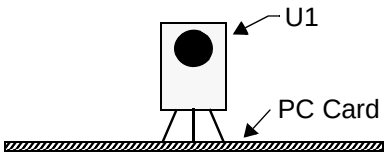


Figure 3-21, U1, IR Interface, Card Edge View

The receiver supports interaction with an Infrared remote control included with your EVM.

Table 32: U1, Infrared Interface

U1 Pin #	MSP430 Signal, Pin #
1	P1.2/TA1/A1+/A4-, U2, Pin 4
2	GND
3	VCC_3V3

3.2.32 SPK1, Speaker Interface

The speaker interface SPK1 provides a speaker output driven directly from the DM365 processor. The connections going to the processor are shown in the table below.

Table 33: SPK1, Speaker Interface

SPK1 Pin #	DM365 Name, Pin #
1	SPP, U18, Pin B9
2	SPN, U18, Pin A9

3.2.33 BHT1, Battery Interface

BHT1 is a holder for a BA2032SM battery. The signals on each pin are shown below in the table below.

Table 34: BHT1, Battery Interface

BHT1 Pin #	BHT1 Connection
1	VBK, Up, Pin 13
2	Ground

3.2.34 M1, Microphone Interface

The microphone interface, M1, provides a microphone input directly into the DM365 processor. The connections going to the processor are shown in the table below.

Table 35: M1, Microphone Interface

M1 Pin #	DM365 Signal Name, Pin #
1	MICIP, U18-9, Pin B8
2	MICIN, U18-9, Pin C9

3.3 LEDs

The EVM has nine (9) LEDs which are located on the top side of the board. Information regarding the LEDs are shown in the table below.

Table 36: LEDs

LED #	Use	Color
DS1	+5 Volts present	Green
DS2	User control via MSP430 I^2C	Green
DS3	User control via MSP430 I^2C	Green
DS4	User control via MSP430 I^2C	Green
DS5	User control via MSP430 I^2C	Green
DS6	User control via MSP430 I^2C	Green
DS7	User control via MSP430 I^2C	Green
DS8	User control via MSP430 I^2C	Green
DS9	User control via MSP430 I^2C	Green

3.4 Switches

The EVM has twenty-three (23) switches. The function of these switches are shown in the table below.

Table 37: Switches

Switch	Function	Type	Silkscreen
SW1	EMU0/EMU1 Control	2 Position DIP	
SW2	PRTSC ON	Push Button/Momentary	PRTSCC
SW3	Non-Supported	Push Button/Momentary	
SW4	Boot/Config Select	6 Position DIP	
SW5	Board Select	6 Position DIP	
SW6	User Readable	Push Button/Momentary	KEY2
SW7	User Readable	Push Button/Momentary	LEFT
SW8	User Readable	Push Button/Momentary	EXIT
SW9	User Readable	Push Button/Momentary	DOWN
SW10	User Readable	Push Button/Momentary	ENTER
SW11	User Readable	Push Button/Momentary	UP
SW12	User Readable	Push Button/Momentary	KEY1
SW13	User Readable	Push Button/Momentary	RIGHT
SW14	User Readable	Push Button/Momentary	MENU
SW15	User Readable	Push Button/Momentary	REC
SW16	User Readable	Push Button/Momentary	REW
SW17	User Readable	Push Button/Momentary	SKIP -
SW18	User Readable	Push Button/Momentary	STOP
SW19	User Readable	Push Button/Momentary	FF
SW20	User Readable	Push Button/Momentary	SKIP +
SW21	Short to Ground	Push Button/Momentary	PLAY PAUSE
SW22	Short to Ground	Push Button/Momentary	
SW23	PRTSC Mode	2 Position DIP	

3.4.1 SW1, EMU0/1 Select Switch

SW1 is a 2 position DIP switch providing 4 options in selecting the state of the EMU0 and EMU1 pins on the TMS320DM365 processor. A view of the switch is shown in the figure below. The selection options with this switch are in the table below.

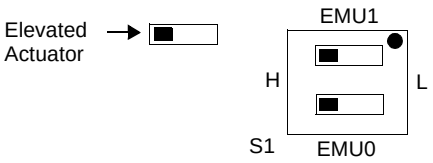


Figure 3-22, SW1, EMU0/1 Select Switch

Table 38: SW1, EMU0/1 Select

State at Reset EMU1	State at Reset EMU0	Function
L(0)	L(0)	Reserved
L(0)	H(1)	Reserved
H(1)	L(0)	Reserved
H(1)	H(1)	ICE PICK Mode * Both ARM & DSP JTAG Enabled

* is the factory shipped configuration

3.4.2 SW2, PWCTRO0 Pushbutton

Switch SW2 is a push button momentary switch that forces the PWCTRO0 signal on the DM365, U18-11, pin J3, to ground when the switch is depressed.

3.4.3 SW3, Non-Supported Pushbutton

Switch SW3 is a not currently used for any function

3.4.4 SW4, Boot Mode / Configuration Select

Switch SW4 is a 6 position DIP switch used to select the ARM Boot Mode and processor configuration. The first 3 positions selection the ARM boot mode. The last 3 positions select the processor configuration. The figure and tables below show these options.

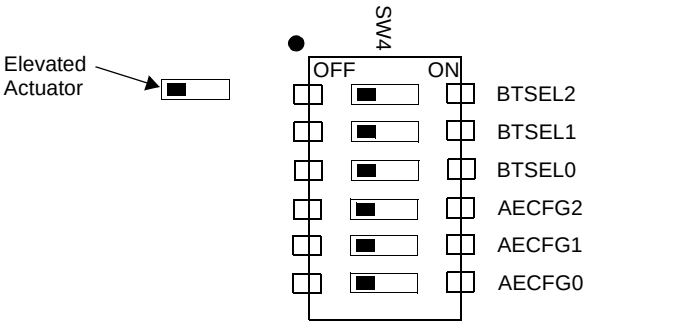


Figure 3-23, SW4, Boot Mode / Configuration Select

Table 39: SW4, Boot Mode Select

Pos 3	Pos 2	Pos 1	HW Code	Boot Mode
ON	ON	ON	0 0 0	NAND Boot *****
ON	ON	OFF	0 0 1	ASYNC EMIF
ON	OFF	ON	0 1 0	MMC/SD Boot
ON	OFF	OFF	0 1 1	UART Boot
OFF	ON	ON	1 0 0	USB Boot
OFF	ON	OFF	1 0 1	SPI Boot
OFF	OFF	ON	1 1 0	EMAC Boot
OFF	OFF	OFF	1 1 1	HPI Boot

Table 40: SW4, Configuration Select

Pos 6	Pos 5	Pos 4	HW Code	Configuration Mode
ON	ON	ON	0 0 0	8-bit AEMIF Configuration *
ON	ON	OFF	0 0 1	16-bit AEMIF Configuration

***** default setting

3.4.5 SW5, Board Configuration Select

Switch SW5 is a 6 position switch that configures specific board functions. The figure below shows the switch as it appears on the EVM.

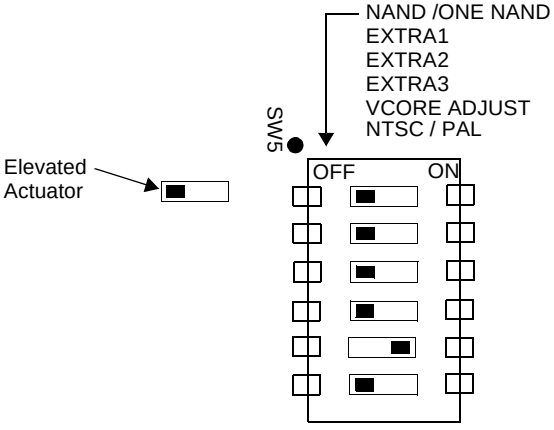


Figure 3-24, SW5, Board Configuration Select

The table below shows the function of each switch position on SW5.

Table 41: SW5, Board Configuration Select

Position	State	Bit Value	Function
1	OFF	0	SELNAND *
	ON	1	SELONENAND
2	OFF	0	Reserved *
	ON	1	Reserved
3	OFF	0	Reserved *
	ON	1	Reserved
4	OFF	0	Reserved *
	ON	1	Reserved
5	OFF	0	Vcore = 1.2 Volts
	ON	1	Vcore = 1.35 Volts *
6	OFF	0	NTSC (CPLD register bit) *
	ON	1	PAL (CPLD register bit)

***** = default

3.4.6 SW6 - SW21, Function Pushbuttons

Switches SW6 through SW21 are push button momentary switches that are inputs in to the DM365 processor. These switches can be read with software and their function is determined by the application.

3.4.7 SW22, MSP430 IO0 Pushbutton

Switch SW22 is a push button momentary switch reserved for future use.

3.4.8 SW23, PRTSC Mode Select

Switch SW23 is a 2 position DIP switch that allows the user to select _____. Only **one** switch should be engaged at a time. The figure below shows the switch as it appears on the EVM.

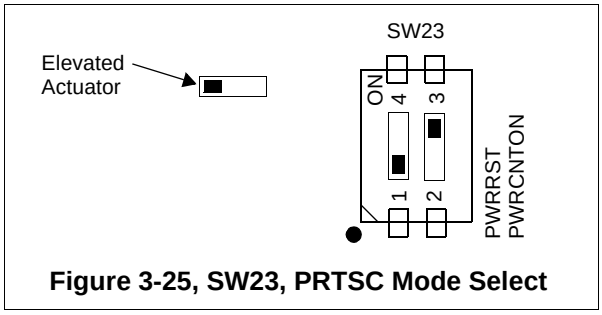


Figure 3-25, SW23, PRTSC Mode Select

The table below shows the setting for SW23.

Table 42: SW23, PRTSC Mode Select

Position #	Signal Name	Function
1 - 4	XRESET pulled high on TPS65510	_____
2 - 3	CS pulled high on TPS65510	_____ *

* default

3.5 Jumpers

The following section describes the jumpers on the DM365 EVM.

3.5.1 JP1, Jumper Block

Jumper block JP1 allows the user to connect signals from the DM365 processor to the TVL320AIC3101, U7. The signals on this 9 x 2 header are shown in the table below.

Table 43: JP1, Jumper Block

Pin #	Signal Name	Pin #	Signal Name
2	AIC_McBSP_CLKX	1	AIC_BCLK, U7, Pin 2
4	AIC_McBSP_CLKR	3	AIC_BCLK, U7, Pin 2
6	AIC_McBSP_FSX	5	AIC_WCLK
8	AIC_McBSP_FSR	7	AIC_WCLK
10	AIC_McBSP_DX	9	AIC_DIN
12	AIC_McBSP_DR	11	AIC_DOUT
14	I2C_DATA	13	SDA, U7, Pin 9
16	I2C_SCLK	15	SDL, U7, Pin 8
18	Ground	17	Ground

3.6 Test Points

The EVM has 55 test points. The following 2 figures identify the position of each test point. The next two tables lists each test point and the signal appearing on that test point.

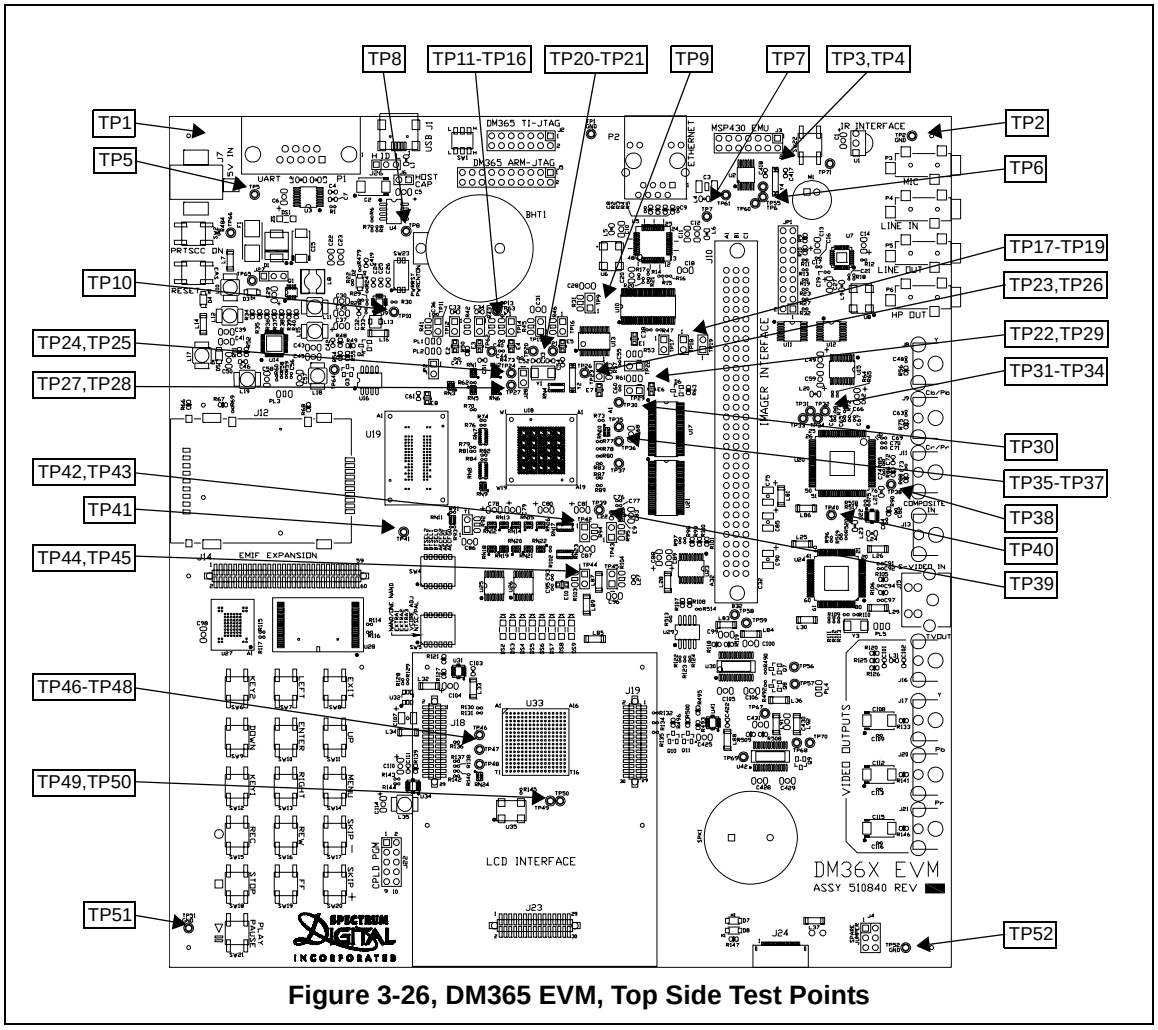


Figure 3-26, DM365 EVM, Top Side Test Points

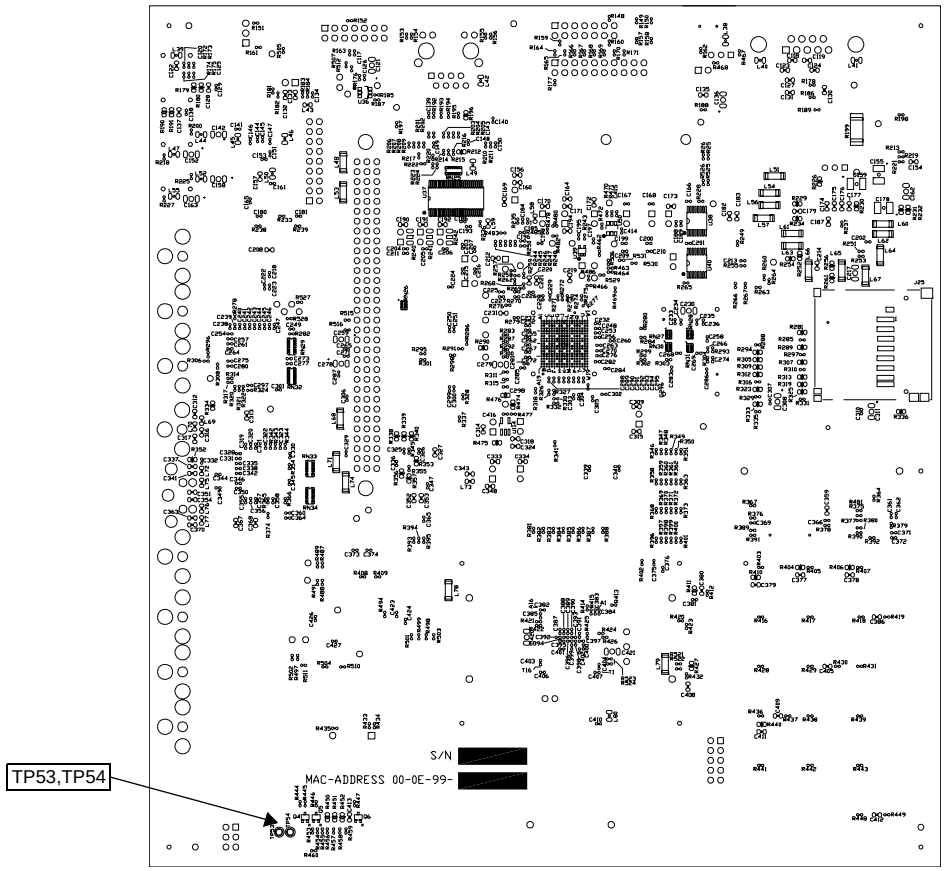


Figure 3-27, DM365 EVM, Bottom Side Test Points

Table 44: DM365 EVM Test Points

Test Point #	Signal	Test Point #	Signal
TP1	GND	TP33	U20, Pin 25, SOGOUT
TP2	GND	TP34	U20, Pin 23, SVSOUT
TP3	MSP430_IO3	TP35	U18-9, C9, LINEO
TP4	MSP430_IO4	TP36	U18-10, A6, ADC_CH5
TP5	VCC_5V	TP37	U18-10, D7, ADC_CH4
TP6	MSP430_IO2	TP38	U20, Pin 80, EXT_CLK
TP7	U5, Pin 25, INT#PHYAD0	TP39	VREF, U18-3, D11
TP8	VCC_3V3, VBUS_OCn2, U4, Pin 5	TP40	GND
TP10	U9, Pin6, PWMON	TP41	GND
TP20	U18-13, L1, MXI1	TP46	U33A, F2, B1.IO_21
TP21	U18-13, K1, MXO1	TP47	U33A, P7, B4.IO_47
TP24	U18-14, R1, RSV1	TP48	U33A, P11, B4.IO_21
TP25	U18-11, K2, PWCTRO0	TP49	U33A, M4, B1.IO_58
TP26	DM360 RESETn, U18-13, H3	TP50	U33A, P2, B1.IO_65
TP27	U18-14, R4, RSV2	TP51	GND
TP28	U18-11, L5, PWCTRO1	TP52	GND
TP30	U18-14, A1, RSV0	TP53	J24, Pin 11,12, BAT_CHG
TP31	U20, Pin 24, HSOUT	TP54	J24, Pin 19
TP32	U20, Pin 22, FIDOUT		

There are 18 power test points on the EVM. These test points provide a convenient mechanism to check the EVM's multiple power supplies. The table below shows the voltages for each test point and what the supply is used for.

Table 45: Power Test Points

Access Test Point	Voltage	Shunt	Power Domain
T1	+1.8V	0.02 ohms	VCC_1V8, U18-14, R12, CPU_VDD_DDR
TP9	+3.3V	0.02 ohms	VCC_3V3, U18-14, P5, CPU_VDDSHV
TP11	+1.2V	0.02 ohms	VCC_1V2, U18-14, R3
TP12	+3.3V	0.02 ohms	VCC_3V3
TP13	+1.8V	0.02 ohms	VCC_1V8
TP14	+1.8V	0.02 ohms	VCC_1V8, U18-14, N4
TP15	+1.2V	0.02 ohms	VCC_1V2, U18-14, J14, CPU_VDD
TP16	+1.8V	0.02 ohms	VCC_1V8, U18-10, G9
TP17	+1.8V	0.02 ohms	VCC_1V8, U18-14, E5
TP18	+1.8V	0.02 ohms	1V8_BB_UP, U18-11, K6
TP19	+1.2V	0.02 ohms	1V2_BB_UP, U18-11, K7,J6
TP22	+1.8V	0.02 ohms	VCC_1V8, U18-9, E9
TP23	+1.8V	0.02 ohms	VCC_1V8, U18-13, L6
TP29	+3.3V	0.02 ohms	VCC_3V3, U18-9, E10
TP42	+3.3V	0.02 ohms	VCC_3V3, U18-14, R14, CPU_VDDSHV10
TP43	+1.8V	0.02 ohms	VCC_1V8, U18-3, D10
TP44	+1.2V	0.02 ohms	VCC_1V2, U18-3, E12
TP45	+1.2V	0.02 ohms	VCC_1V2, U18-14, M14, CPU_VDDS

Appendix A

Schematics

This appendix contains the schematics for the DM365 EVM.

REV	DESCRIPTION	DATE	APPROVED
A	Initial schematic ready for layout - Alpha Release	03/04/08	RRP
B	Updates for initial prototype build	09/24/08	RRP
C	BETA Release	10/30/08	RRP

SCHEMATIC CONTENTS

SHEET01 - TITLE SHEET
SHEET02 - DM365 DDR2 INTERFACE
SHEET03 - DM365 EMIF/BOOT MODES/CFG MODES
SHEET04 - DM365 USB
SHEET05 - DM365 VIDEO PORT IN
SHEET06 - DM365 VIDEO PORT OUT
SHEET07 - DM365 ANALOG VIDEO OUT
SHEET08 - DM365 SD/MMC/MS IF
SHEET09 - DM365 I/O
SHEET10 - DM365 JTAG,CLKS,RESET
SHEET11 - DM365 ADC
SHEET12 - DM365 MIC/SPEAKER
SHEET13 - DM365 POWER PINS
SHEET14 - DM365 POWER CONTROL
SHEET15 - DM365 GROUND PINS
SHEET16 - DM365 DECOUPLING CAPS
SHEET17 - DDR2 MEMORY
SHEET18 - USB INTERFACE CONNECTOR
SHEET19 - JTAG CONNECTORS
SHEET20 - CPLD BANK A
SHEET21 - CPLD BANK B
SHEET22 - CPLD BANK C
SHEET23 - CPLD BANK D
SHEET24 - CLPD POWER
SHEET25 - HOST/EMIF DC INTERFACE
SHEET26 - NAND FLASH
SHEET27 - ONE NAND
SHEET28 - I2C/SPI EEPROM
SHEET29 - RS232 INTERFACE
SHEET30 - SD/MMC/MS IF
SHEET31 - SD.MMC IF 2
SHEET32 - VIDEO COMPONENT OUT
SHEET33 - VIDEO INPUT MULTIPLEXER
SHEET34 - VIDEO INPUT DC CONNECTORS
SHEET35 - TVP7002
SHEET36 - HD VIDEO IN CONNECTORS
SHEET37 - TVP5146 DECODER
SHEET38 - McBSP MUX
SHEET39 - AIC3101
SHEET40 - VIDEO DC OUTPUT CONNECTORS
SHEET41 - DILC HOST CONNECTOR
SHEET42 - ETHERNET MUX
SHEET43 - ETHERNET PHY
SHEET44 - MSP430 IR CONTROLLER
SHEET45 - SWITCHES
SHEET46 - LEDS
SHEET47- POWER SUPPLY TPS65510
SHEET48 - POWER SUPPLY TPS65530
SHEET49 - POWER SUPPLY
SHEET50 - DECODER 3V3,1V8 POWER
SHEET51 - ALT CPU CORE POWER
SHEET52 - ALT 3V3 POWER
SHEET53 - POWER IN

I2C ADDRESS	Device
0x18	AIC3101
0x25	MSP430
0x2C	THS7303
0x2E	THS7353
0x50	CAT24C256
0x5D	TVP5146
0x5C	TVP7002

REVISION STATUS OF EVM		
Assembly	510840-0001	C
PWB	510841-0001	C
LOGIC	510842-0001	C

REVISION STATUS OF SHEETS

REV	C	C	C							
SHEET	51	52	53							
REV	C	C	C	C	C	C	C	C	C	C
SHEET	41	42	43	44	45	46	47	48	49	50
REV	C	C	C	C	C	C	C	C	C	C
SHEET	31	32	33	34	35	36	37	38	39	40
REV	C	C	C	C	C	C	C	C	C	C
SHEET	21	22	23	24	25	26	27	28	29	30
REV	C	C	C	C	C	C	C	C	C	C
SHEET	11	12	13	14	15	16	17	18	19	20
REV	C	C	C	C	C	C	C	C	C	C
SHEET	1	2	3	4	5	6	7	8	9	10

NEXT ASSY	USED ON
APPLICATION	

		DATE
DWN	R.R.P.	03/04/2008
CHK	T.W.K.	03/04/2008
ENGR	R.R.P.	03/04/2008
ENGR-MGR	R.R.P.	03/04/2008
QA	C.M.D.	03/04/2008
MFG	R.R.P.	03/04/2008
RLSE	R.R.P.	03/04/2008

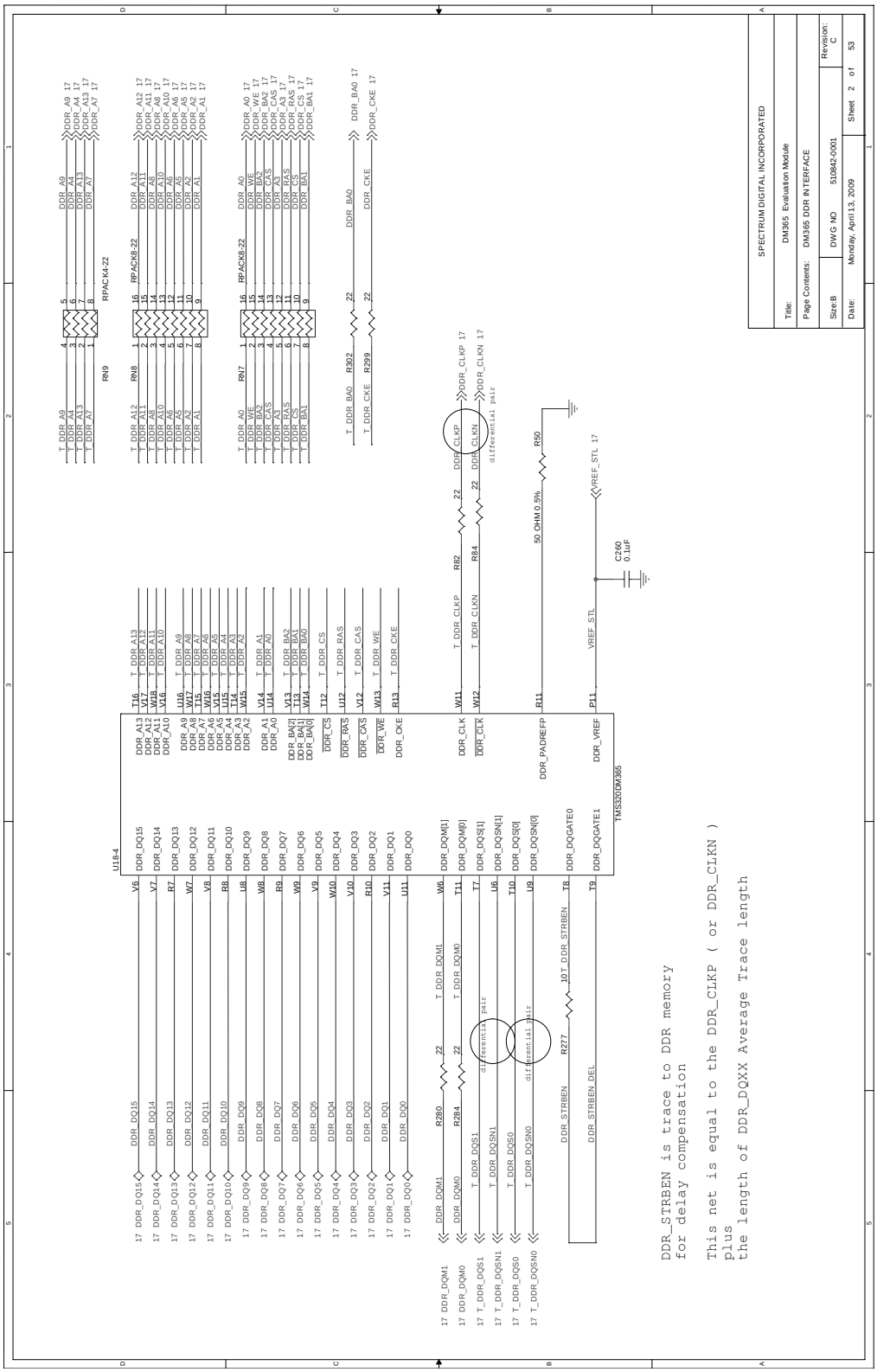
SPECTRUM DIGITAL INCORPORATED

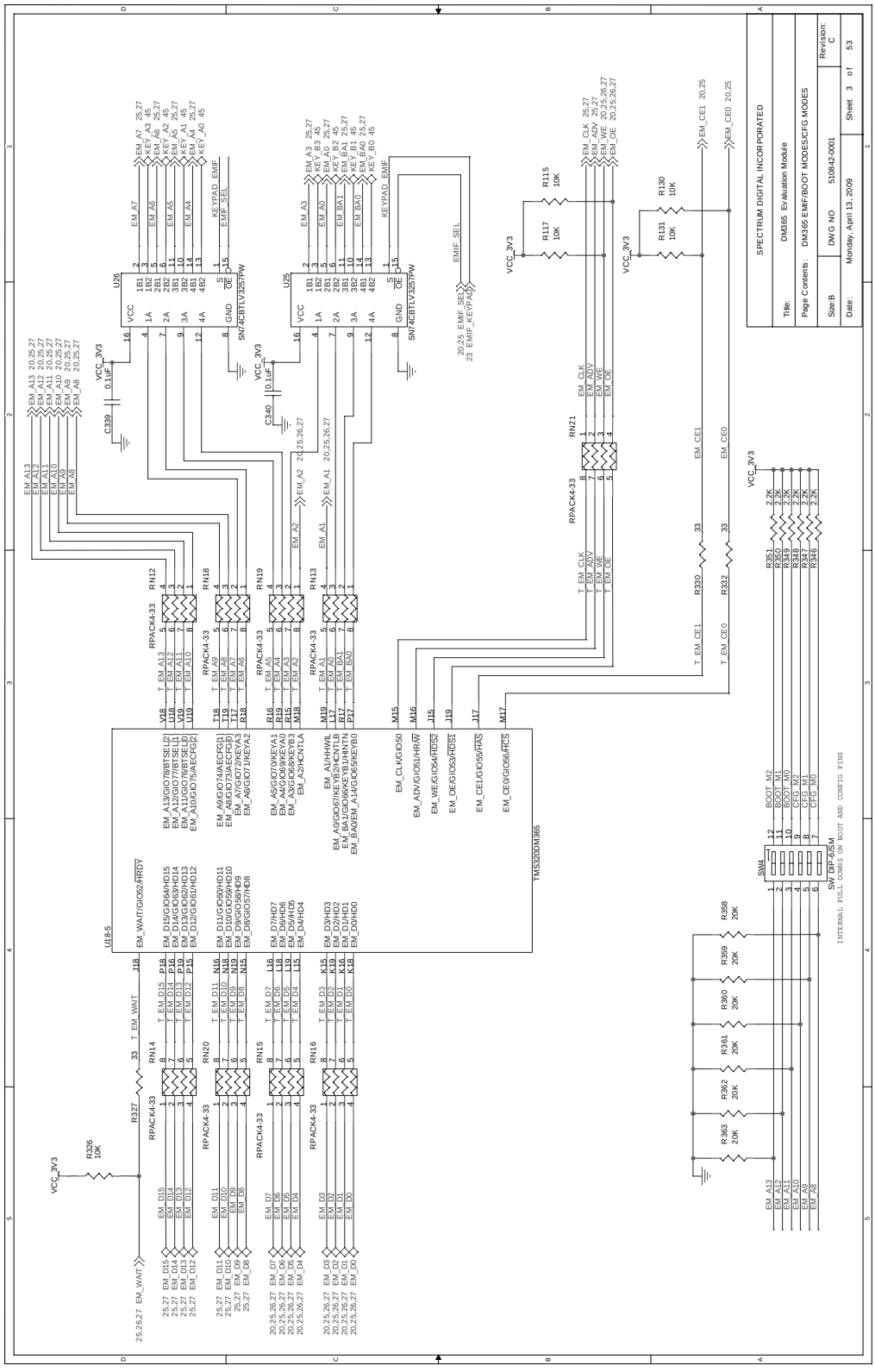
Title: DM365 Evaluation Module

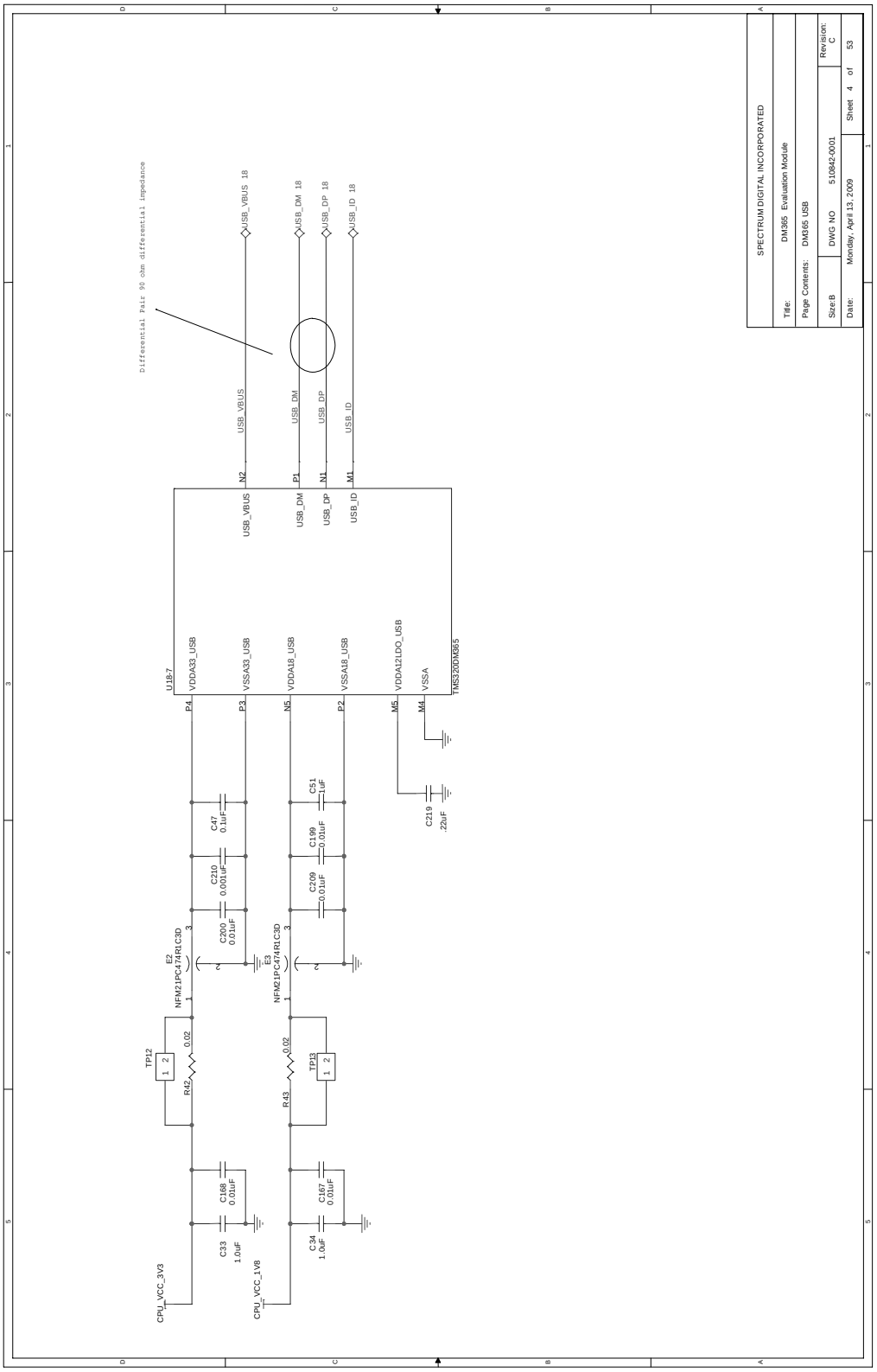
Page Contents: TITLE SHEET

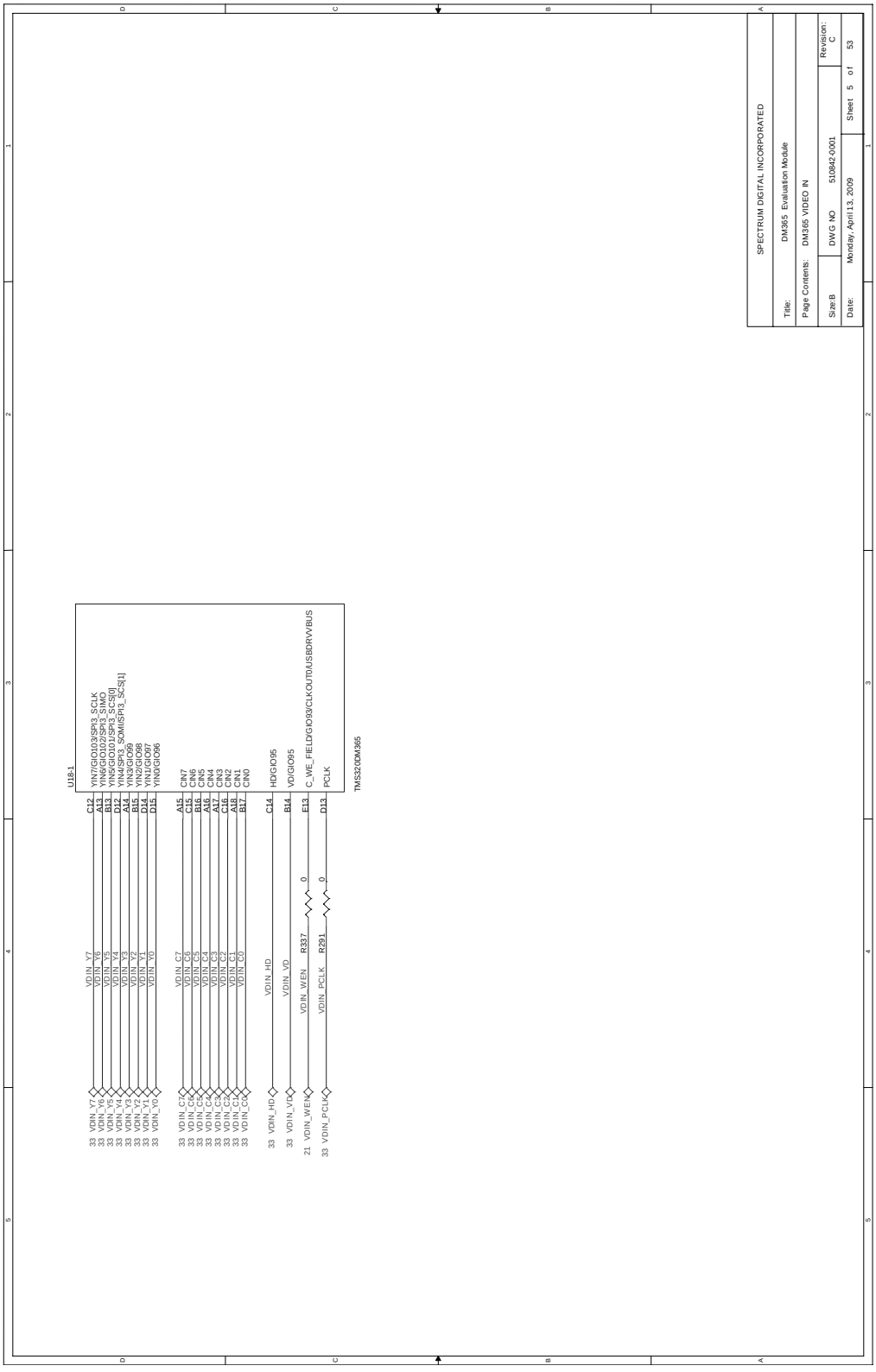
Size:B DWG NO 510842-0001 Revision: C

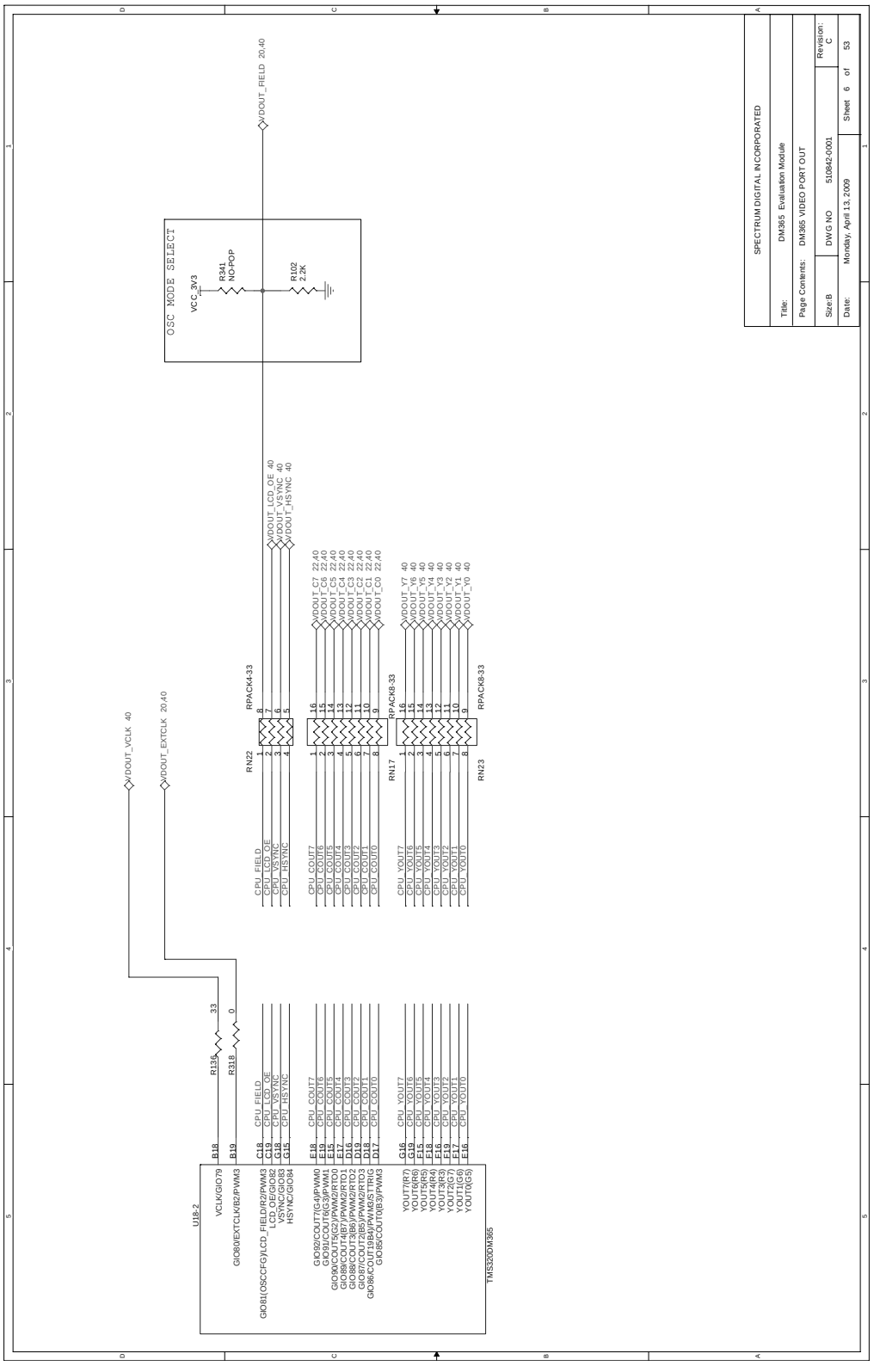
Date: Monday, April 13, 2009 Sheet 1 of 53

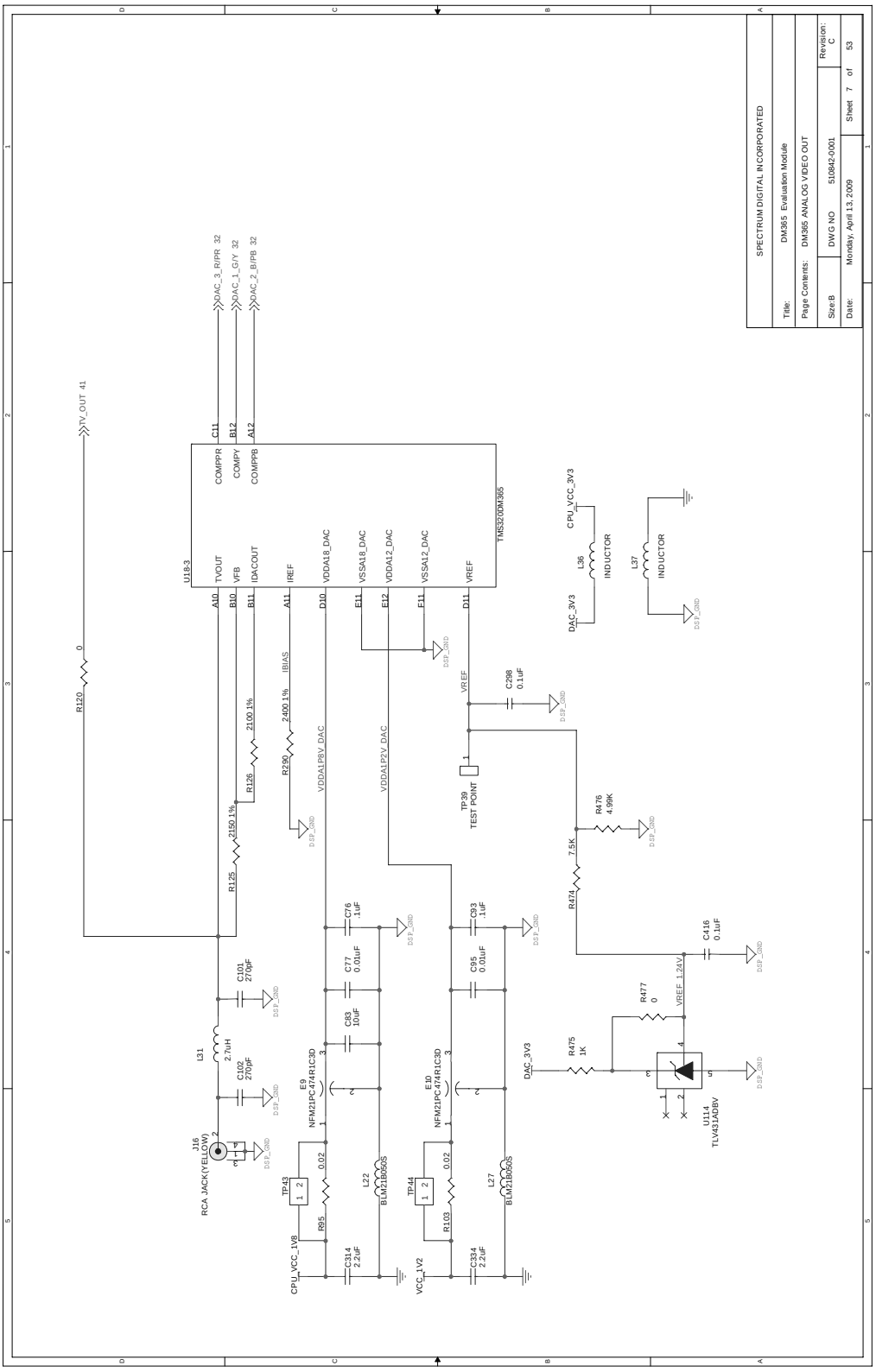

SPECTRUM DIGITAL INCORPORATED
Title: DM365 Evaluation Module
Page Contents: DM365 DDR INTERFACE
Size: B
DWG NO 510842-0001
Revision: C
Date: Monday, April 13, 2009
Sheet 2 of 53
TMS320DM365
RPACK4-22
RPACK8-22
DDR_STRBEN is trace to DDR memory
for delay compensation
This net is equal to the DDR_CLKP (or DDR_CLKN)
plus
the length of DDR_DQXX Average Trace length

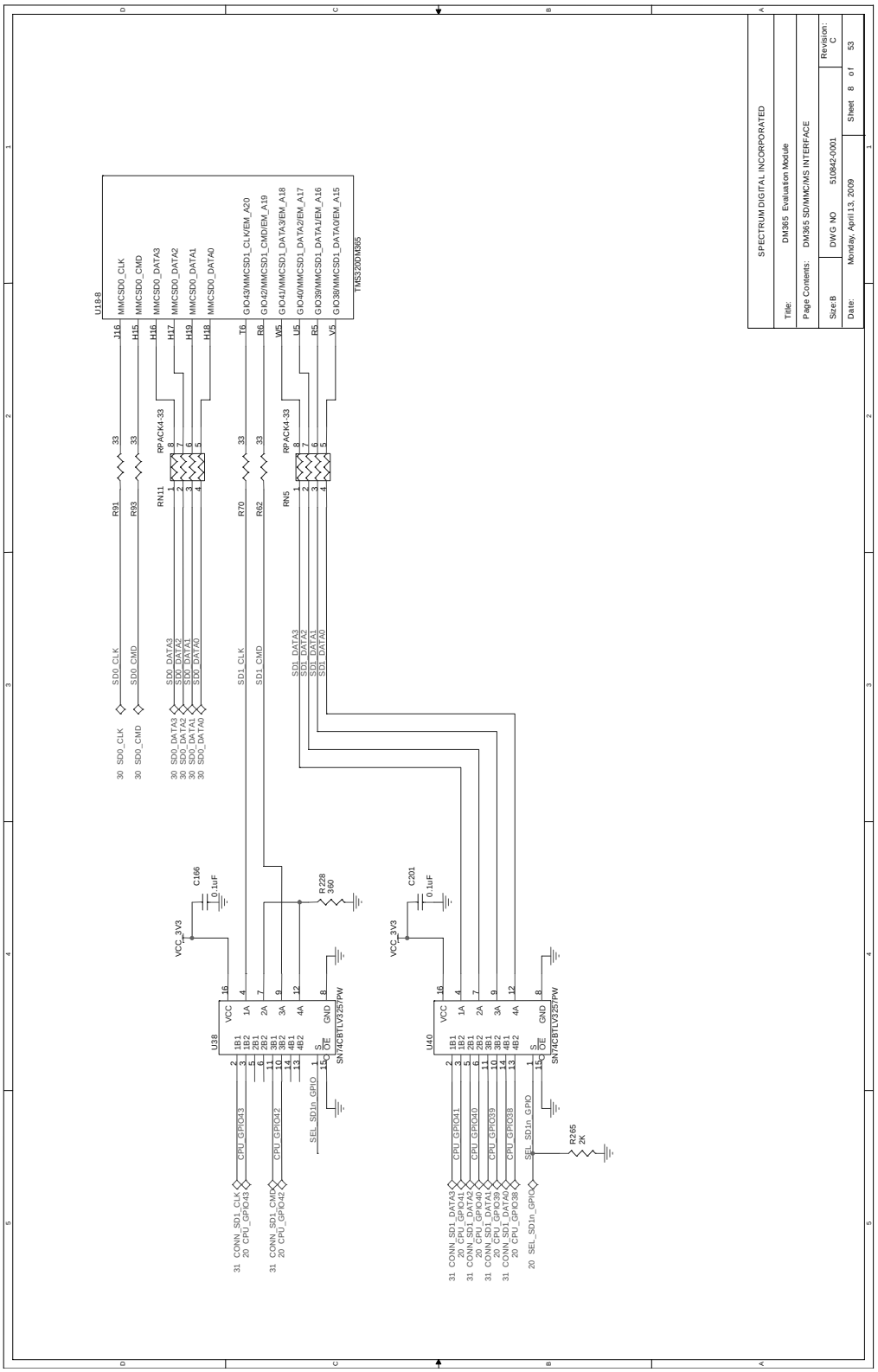

SPECTRUM DIGITAL INCORPORATED
Title: DM365 Evaluation Module
Page Contents: DM365 EMIF/BOOT MODES/CFG MODES
Size: B
DWG NO 5108142-0001
Revision: C
Date: Monday, April 13, 2009
Sheet 3 of 53
TMS320DM365
SW4
SW_DIP-4/SM
INTERNAL PULL-UP/DN FOR BOOT AND CONFIG PINS
SN74CBTLV3257PW
RPACK4-33

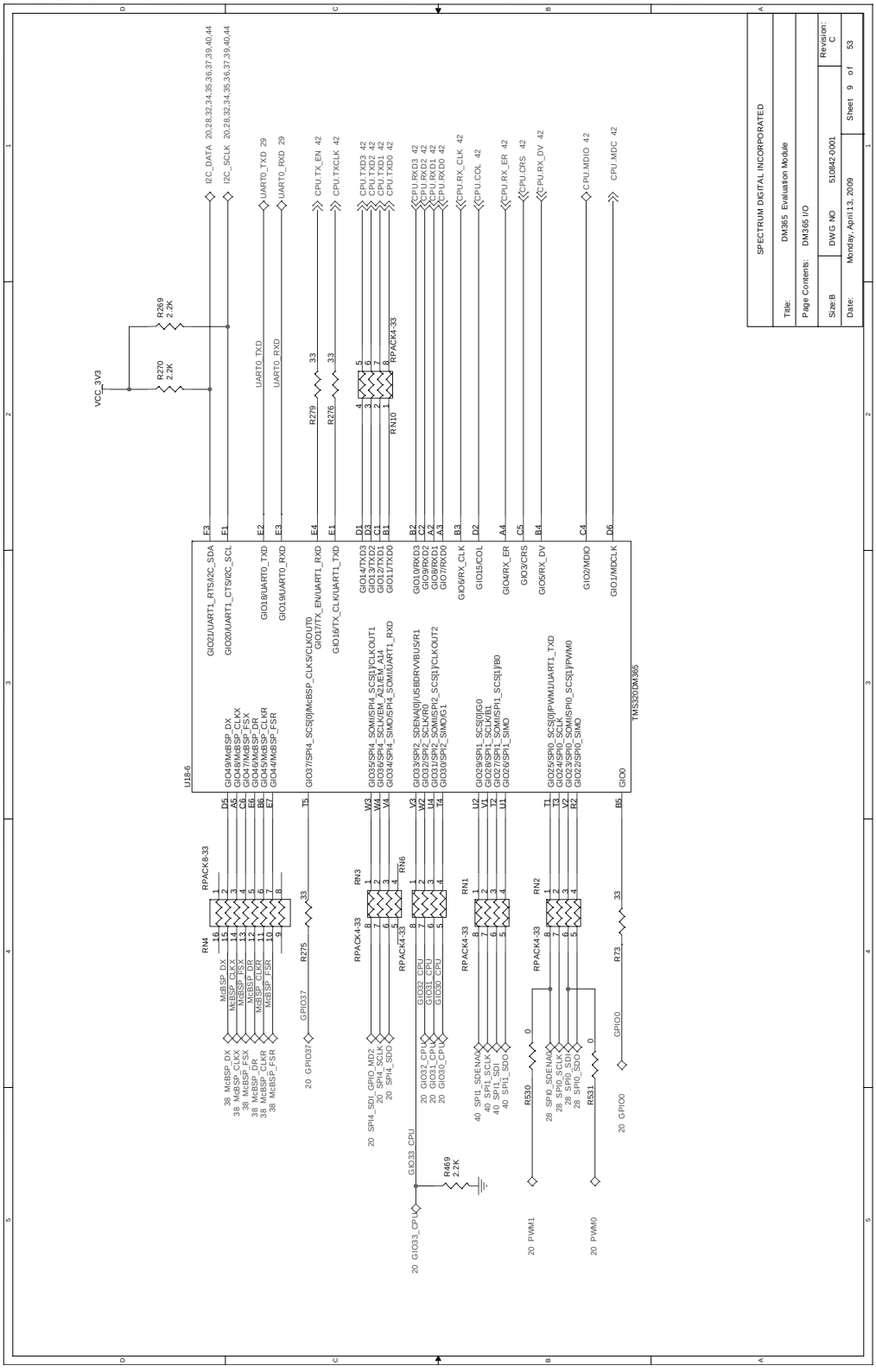

SPECTRUM DIGITAL INCORPORATED
Title: DM365 Evaluation Module
Page Contents: DM365 USB
Size:B
DWG NO 510842-0001
Revision: C
Date: Monday, April 13, 2009
Sheet 4 of 53
Differential Pair 90 ohm differential impedance
USB_VBUS 18
USB_DM 18
USB_DP 18
USB_ID 18
USB_VBUS
USB_DM
USB_DP
USB_ID
N2
P1
N1
M1
U18-7
VDDA33_USB
VSSA33_USB
VDDA18_USB
VSSA18_USB
VDDA12LDO_USB
VSSA
TMS320DM365
P4
P3
N5
P2
M5
M4
C47 0.1uF
C210 0.001uF
C200 0.01uF
C51 1uF
C199 0.01uF
C209 0.01uF
C219 .22uF
E2
NFM21PC474R1C3D
E3
NFM21PC474R1C3D
TP12
TP13
R42 0.02
R43 0.02
C168 0.01uF
C167 0.01uF
C33 1.0uF
C34 1.0uF
CPU_VCC_3V3
CPU_VCC_1V8

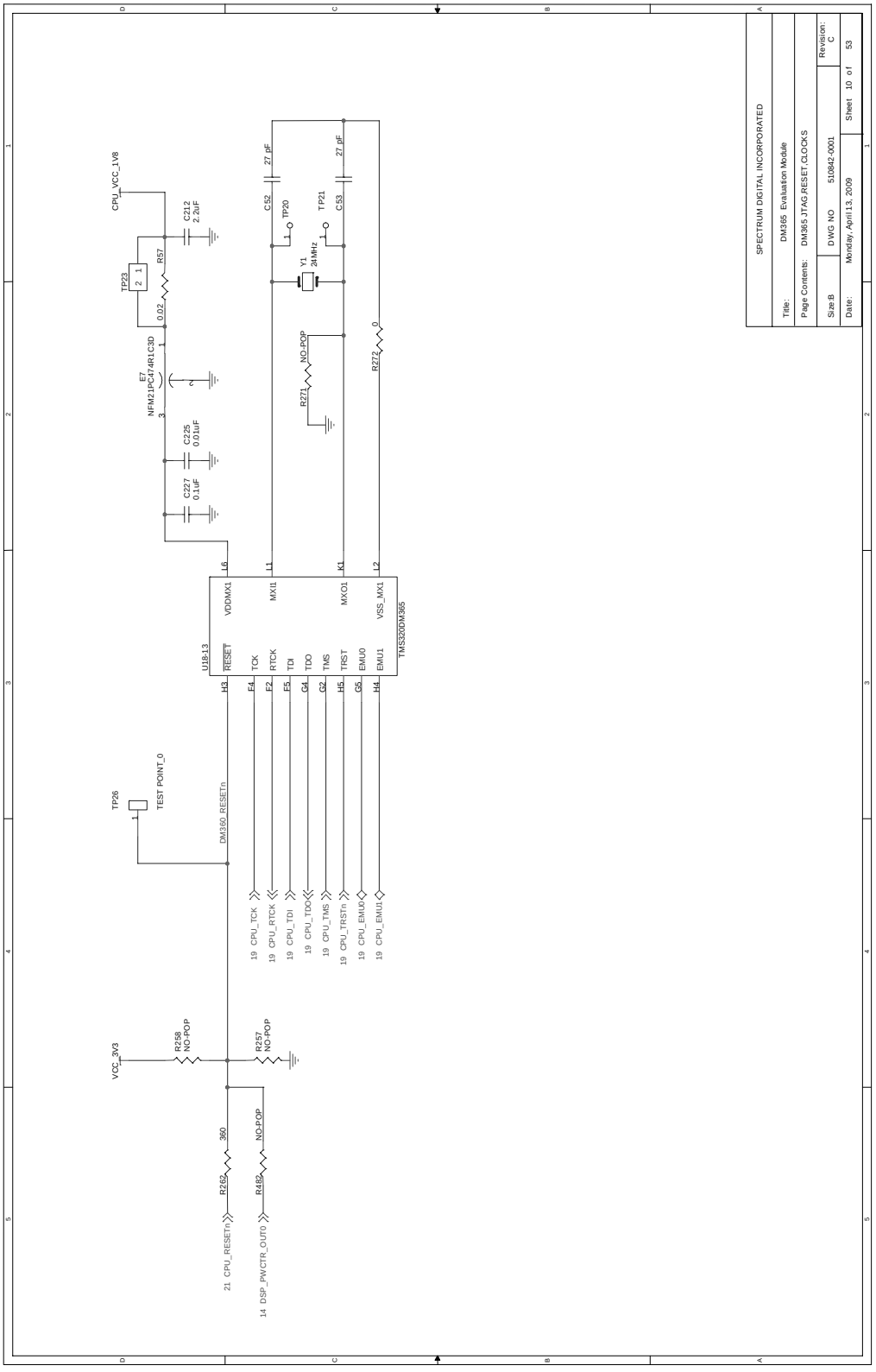

SPECTRUM DIGITAL INCORPORATED
Title: DM365 Evaluation Module
Page Contents: DM365 VIDEO IN
Size: B
DWG NO 510842-0001
Revision: C
Date: Monday, April 13, 2009
Sheet 5 of 53
U18-1
TMS320DM365
VDIN_Y7
VDIN_Y6
VDIN_Y5
VDIN_Y4
VDIN_Y3
VDIN_Y2
VDIN_Y1
VDIN_Y0
VDIN_C7
VDIN_C6
VDIN_C5
VDIN_C4
VDIN_C3
VDIN_C2
VDIN_C1
VDIN_C0
VDIN_HD
VDIN_VD
VDIN_WEN
VDIN_PCLK
R337
R291
0
0

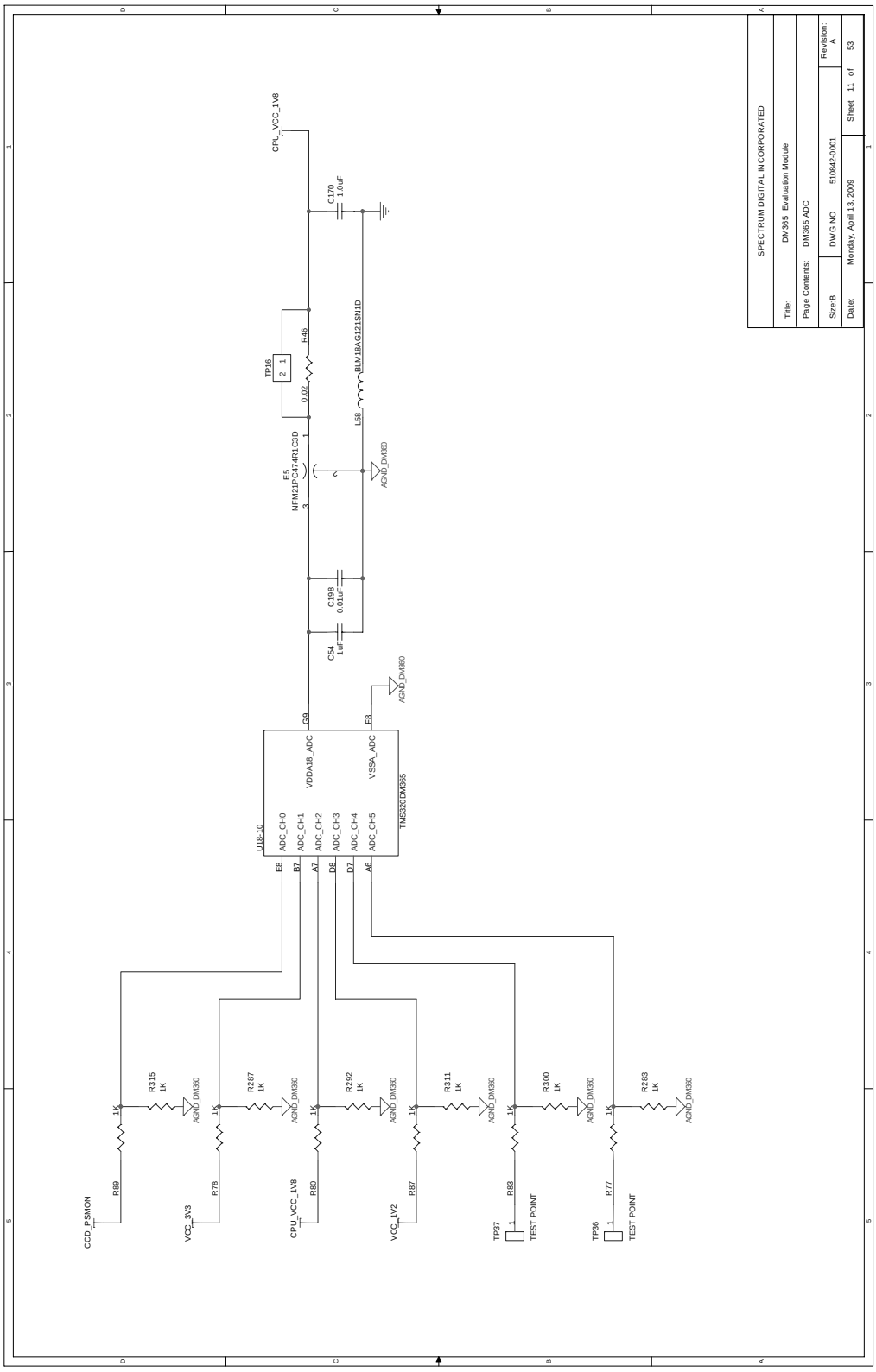

SPECTRUM DIGITAL INCORPORATED
Title: DM365 Evaluation Module
Page Contents: DM365 VIDEO PORT OUT
Size:B
DWG NO 510842-0001
Revision: C
Date: Monday, April 13, 2009
Sheet 6 of 53
OSC MODE SELECT
VCC_3V3
R341 NO-POP
R102 2.2K
VDOUT_FIELD 20,40
VDOUT_VCLK 40
VDOUT_EXTCLK 20,40
VDOUT_LCD_OE 40
VDOUT_VSYNC 40
VDOUT_HSYNC 40
RN22
RPACK4-33
RN17
RPACK8-33
RN23
RPACK8-33
R135 33
R318 0
U18-2
TMS320DM365
CPU_FIELD
CPU_LCD_OE
CPU_VSYNC
CPU_HSYNC
CPU_COUT7
CPU_COUT6
CPU_COUT5
CPU_COUT4
CPU_COUT3
CPU_COUT2
CPU_COUT1
CPU_COUT0
CPU_YOUT7
CPU_YOUT6
CPU_YOUT5
CPU_YOUT4
CPU_YOUT3
CPU_YOUT2
CPU_YOUT1
CPU_YOUT0

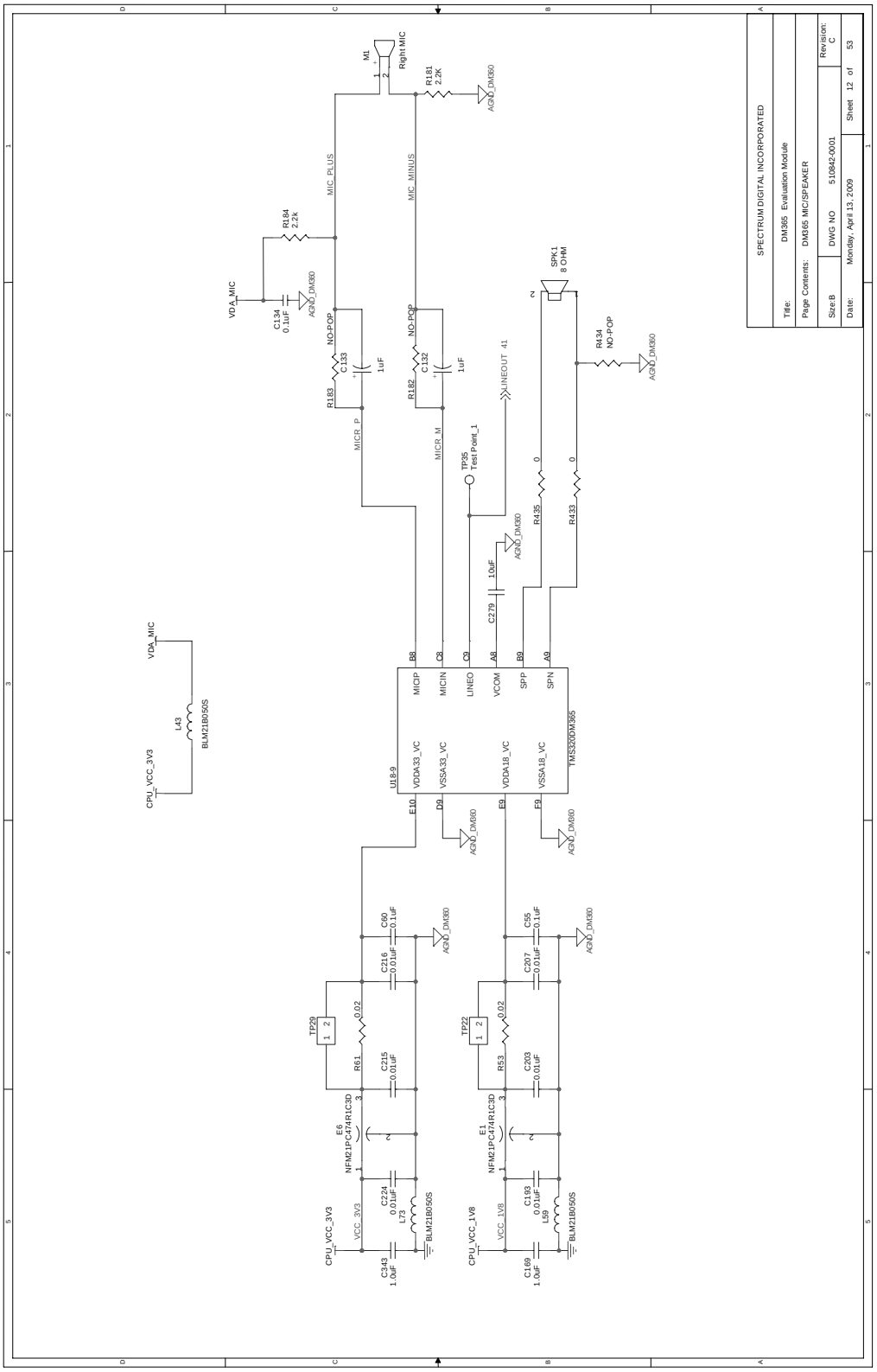

SPECTRUM DIGITAL INCORPORATED
Title: DM365 Evaluation Module
Page Contents: DM365 ANALOG VIDEO OUT
Size:B
DWG NO 510842-0001
Revision: C
Date: Monday, April 13, 2009
Sheet 7 of 53
TV_OUT 41
DAC_3_R/PR 32
DAC_1_G/Y 32
DAC_2_B/PB 32
U18-3
TMS320DM365
TVOUT
VFB
IDACOUT
IREF
COMPPR
COMPY
COMPPB
VDDA18_DAC
VSSA18_DAC
VDDA12_DAC
VSSA12_DAC
VREF
R120 0
R126 2100 1%
R290 2400 1% IBIAS
R125 2150 1%
VDDA1P8V_DAC
VDDA1P2V_DAC
C288 0.1uF
TP39 TEST POINT
R474 7.5K
R476 4.99K
CPU_VCC_3V3
DAC_3V3
L36 INDUCTOR
L37 INDUCTOR
C416 0.1uF
R477 0
VREF_1.24V
R475 1K
U114 TLV431ADBV
C76 .1uF
C77 0.01uF
C93 .1uF
C95 0.01uF
C80 10uF
C101 270pF
C102 270pF
L31 2.7uH
J16 RCA JACK(YELLOW)
E9 NFM21PC474R1C3D
E10 NFM21PC474R1C3D
TP43
TP44
R95 0.02
R103 0.02
L22 BLM21B050S
L27 BLM21B050S
C314 2.2uF
C334 2.2uF
CPU_VCC_1V8
VCC_1V2
DSP_GND

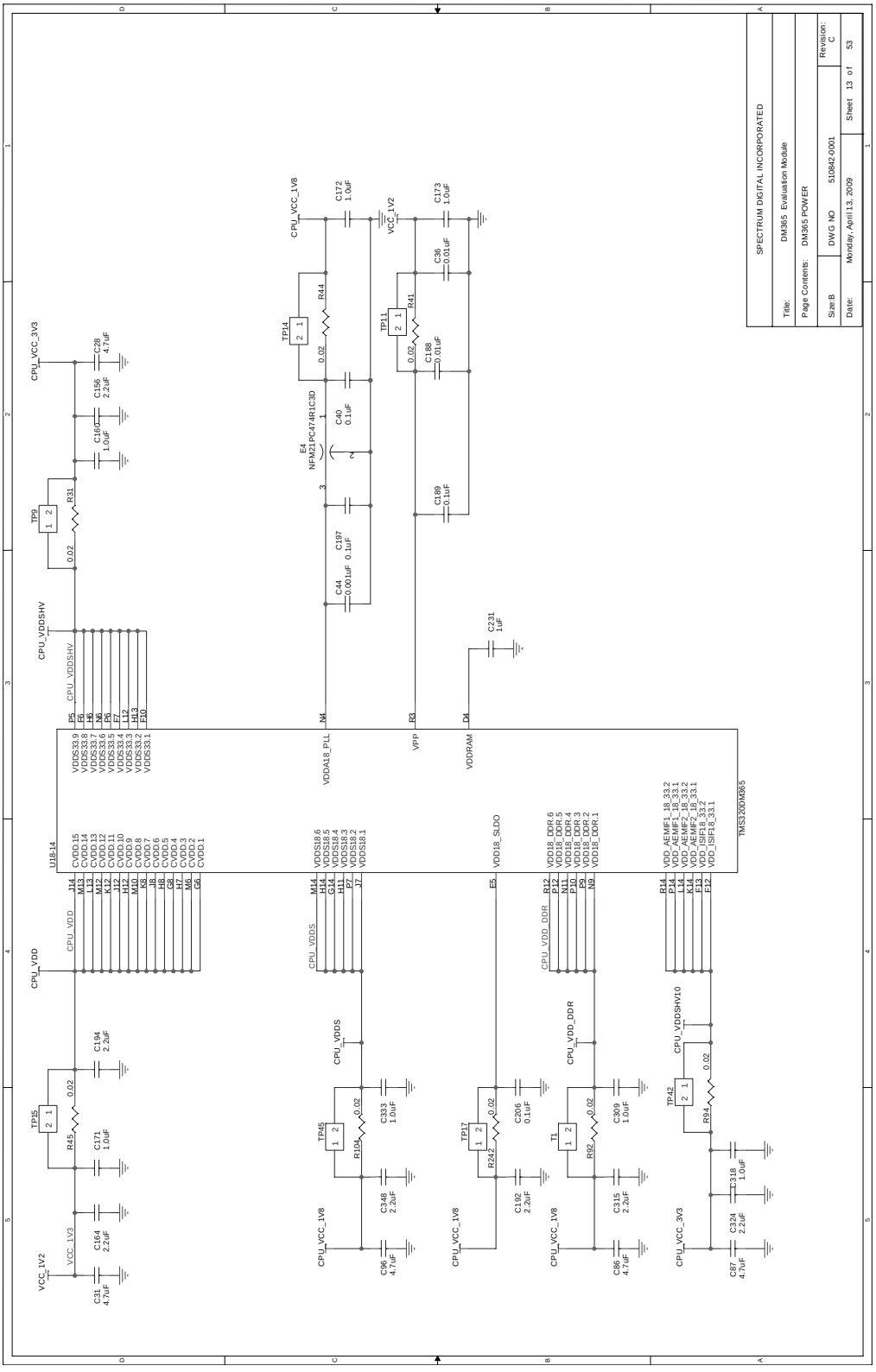

SPECTRUM DIGITAL INCORPORATED
Title: DM365 Evaluation Module
Page Contents: DM365 SD/MMC/MS INTERFACE
Size:B
DWG NO 510842-0001
Revision: C
Date: Monday, April 13, 2009
Sheet 8 of 53
U19-8
MMCSD0_CLK
MMCSD0_CMD
MMCSD0_DATA3
MMCSD0_DATA2
MMCSD0_DATA1
MMCSD0_DATA0
GIO43/MMCSD1_CLK/EM_A20
GIO42/MMCSD1_CMD/EM_A19
GIO41/MMCSD1_DATA3/EM_A18
GIO40/MMCSD1_DATA2/EM_A17
GIO39/MMCSD1_DATA1/EM_A16
GIO38/MMCSD1_DATA0/EM_A15
TMS320DM365
R91
R93
RN11
RPACK4-33
R70
R62
RN5
SD0_CLK
SD0_CMD
SD0_DATA3
SD0_DATA2
SD0_DATA1
SD0_DATA0
SD1_CLK
SD1_CMD
SD1_DATA3
SD1_DATA2
SD1_DATA1
SD1_DATA0
C166
0.1uF
C201
R228
360
R265
2K
VCC_3V3
U38
U40
SN74CBTLV3257PW
CPU_GPIO43
CPU_GPIO42
CPU_GPIO41
CPU_GPIO40
CPU_GPIO39
CPU_GPIO38
SEL_SD1n_GPIO
CONN_SD1_CLK
CONN_SD1_CMD
CONN_SD1_DATA3
CONN_SD1_DATA2
CONN_SD1_DATA1
CONN_SD1_DATA0

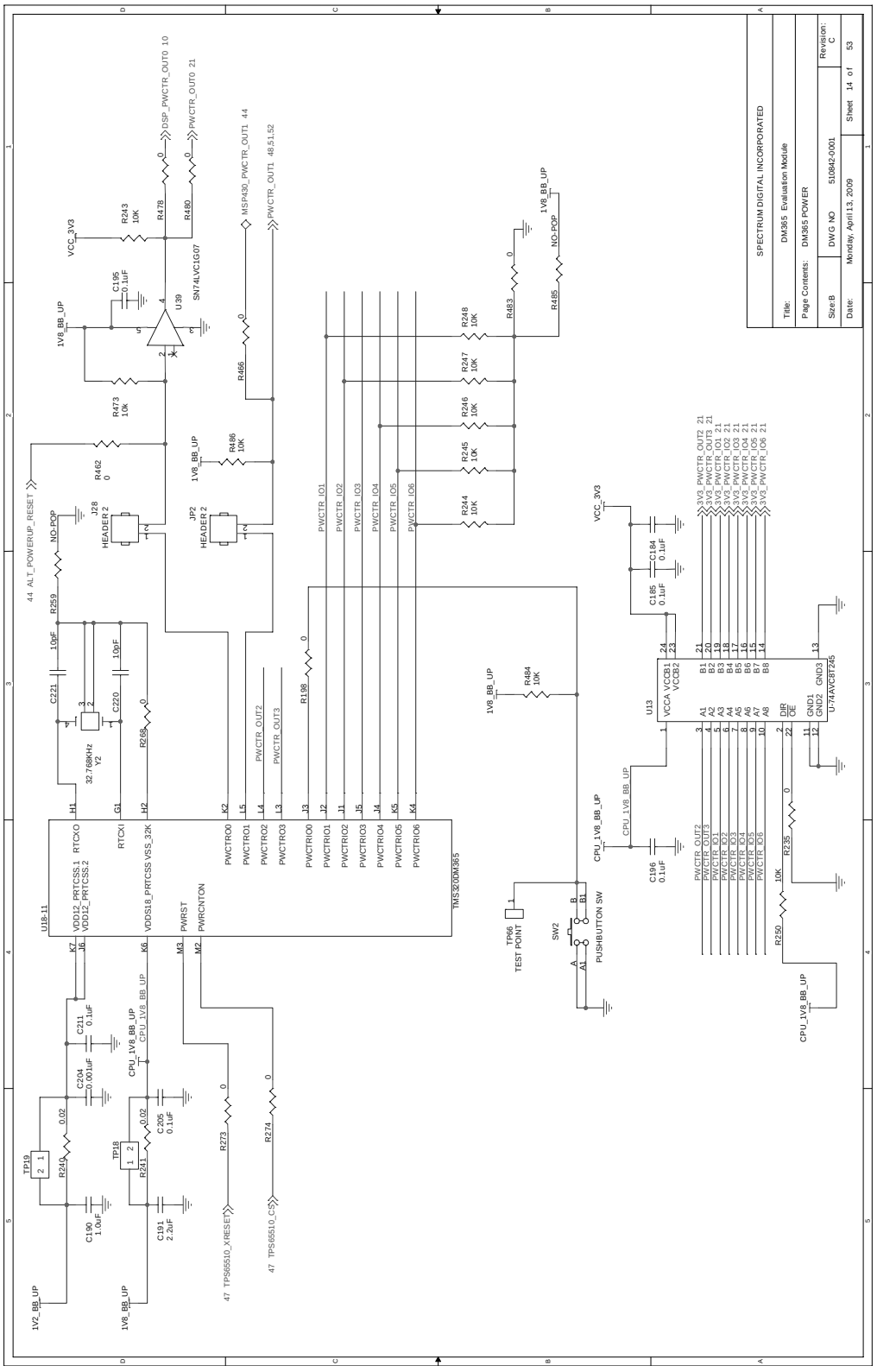

SPECTRUM DIGITAL INCORPORATED
Title: DM365 Evaluation Module
Page Contents: DM365 I/O
Size: B
DWG NO 510842-0001
Revision: C
Date: Monday, April 13, 2009
Sheet 9 of 53
TMS320DM365
U18-6
VCC_3V3
R269 2.2K
R270 2.2K
R279 33
R276 33
RN10 RPACK4-33
RN4 RPACK8-33
RN3 RPACK4-33
RN6 RPACK4-33
RN1 RPACK4-33
RN2 RPACK4-33
R275 33
R73 33
R530 0
R531 0
R469 2.2K
I2C_DATA
I2C_SCLK
UART0_TXD
UART0_RXD
CPU.TX_EN
CPU.TXCLK
CPU.TXD3
CPU.TXD2
CPU.TXD1
CPU.TXD0
CPU.RXD3
CPU.RXD2
CPU.RXD1
CPU.RXD0
CPU.RX_CLK
CPU.COL
CPU.RX_ER
CPU.CRS
CPU.RX_DV
CPU.MDIO
CPU.MDC
McBSP_DX
McBSP_CLKX
McBSP_FSX
McBSP_DR
McBSP_CLKR
McBSP_FSR
GPIO37
GIO33_CPU
GPIO0
PWM1
PWM0
SPI1_SDENA0
SPI1_SCLK
SPI1_SDI
SPI1_SDO
SPI0_SDENA0
SPI0_SCLK
SPI0_SDI
SPI0_SDO
SPI4_SDI
SPI4_SCLK
SPI4_SDO
GPIO_MD2

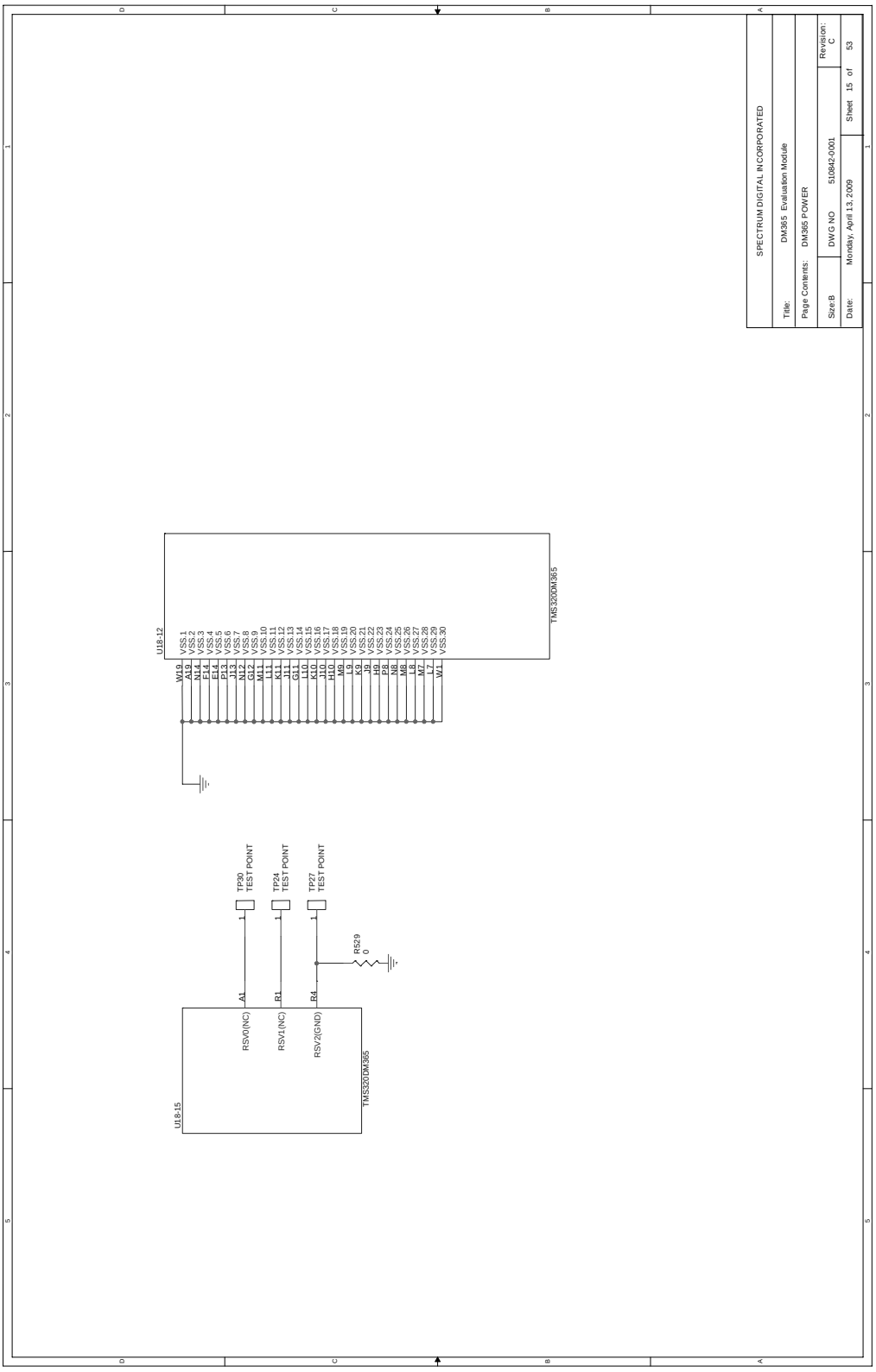

SPECTRUM DIGITAL INCORPORATED
Title: DM365 Evaluation Module
Page Contents: DM365 JTAG,RESET,CLOCKS
Size:B DWG NO 510842-0001 Revision: C
Date: Monday, April 13, 2009 Sheet 10 of 53
CPU_VCC_1V8
C212 2.2uF
R57 0.0Z
TP23
E7 NFM21PC474R1C3D
C225 0.01uF
C227 0.1uF
C52 27 pF
C53 27 pF
TP20
TP21
Y1 24MHz
R271 NO-POP
R272 0
U18-13 TMS320DM365
RESET
VDDMX1
MXI1
MXO1
VSS_MX1
TCK
RTCK
TDI
TDO
TMS
TRST
EMU0
EMU1
TP26 TEST POINT_0
DM360_RESETn
19 CPU_TCK
19 CPU_RTCK
19 CPU_TDI
19 CPU_TDO
19 CPU_TMS
19 CPU_TRSTn
19 CPU_EMU0
19 CPU_EMU1
VCC_3V3
R258 NO-POP
R257 NO-POP
R265 360
R485 NO-POP
21 CPU_RESETn
14 DSP_PWCTR_OUT0


SPECTRUM DIGITAL INCORPORATED
Title: DM365 Evaluation Module
Page Contents: DM365 ADC
Size:B
DWG NO 510842-0001
Revision: A
Date: Monday, April 13, 2009
Sheet 11 of 53
CPU_VCC_1V8
C170 1.0uF
TP16
R46 0.02
BLM18AG121SN1D
L58
E5 NFM21PC474R1C3D
AGND_DM365
C198 0.01uF
C54 1uF
U18-10
TMS320DM365
VDDA18_ADC
VSSA_ADC
ADC_CH0
ADC_CH1
ADC_CH2
ADC_CH3
ADC_CH4
ADC_CH5
R315 1K
R287 1K
R292 1K
R311 1K
R300 1K
R283 1K
R89 1K
R78 1K
R80 1K
R87 1K
R83 1K
R77 1K
CCD_PSMON
VCC_3V3
CPU_VCC_1V8
VCC_1V2
TP37
TP36
TEST POINT


SPECTRUM DIGITAL INCORPORATED
Title: DM365 Evaluation Module
Page Contents: DM365 MIC/SPEAKER
Size:B DWG NO 510842-0001 Revision: C
Date: Monday, April 13, 2009 Sheet 12 of 53
M1
Right MIC
R181 2.2K
R184 2.2k
MIC_PLUS
MIC_MINUS
VDA_MIC
C134 0.1uF
NO-POP
C133 1uF
C132 1uF
R183
R182
MICR_P
MICR_M
LINEOUT 41
SPK1 8 OHM
R434 NO-POP
TP35 TestPoint_1
R435 0
R433 0
C279 10uF
U18-9
TMS320DM365
MICIP
MICIN
LINEO
VCOM
SPP
SPN
VDDA33_VC
VSSA33_VC
VDDA18_VC
VSSA18_VC
L43 BLM21B050S
CPU_VCC_3V3
AGND_DM360
TP29
TP22
R61 0.02
R53 0.02
C60 0.1uF
C216 0.01uF
C215 0.01uF
C55 0.1uF
C207 0.01uF
C203 0.01uF
E6 NFM21PC474R1C3D
E1 NFM21PC474R1C3D
C224 0.01uF
C193 0.01uF
L73 BLM21B050S
L59 BLM21B050S
VCC_3V3
VCC_1V8
C343 1.0uF
C169 1.0uF


SPECTRUM DIGITAL INCORPORATED
Title: DM365 Evaluation Module
Page Contents: DM365 POWER
Size: B
DWG NO 510842-0001
Revision: C
Date: Monday, April 13, 2009
Sheet 13 of 53
U18-14
TMS320DM365
CPU_VCC_1V8
CPU_VCC_3V3
CPU_VDDSHV
CPU_VDD
CPU_VDDS
CPU_VDD_DDR
CPU_VDDSHV10
VCC_1V2
VCC_1V3
VDDA18_PLL
VPP
VDDRAM
VDD18_SLDO
E4
NFM21PC474R1C3D
TP2
TP3
TP5
TP11
TP14
TP17
TP42
TP45
T1
R31
R41
R44
R45
R104
R242
R92
R94
C28
C31
C36
C40
C44
C87
C96
C102
C156
C160
C164
C171
C172
C173
C188
C189
C194
C197
C206
C231
C309
C315
C318
C324
C333
C348


SPECTRUM DIGITAL INCORPORATED
Title: DM365 Evaluation Module
Page Contents: DM365 POWER
Size:B
DWG NO 510842-0001
Revision: C
Date: Monday, April 13, 2009
Sheet 14 of 53
U18-11
TMS320DM365
RTCXO
RTCXI
VDD12_PRTCSS1
VDD12_PRTCSS2
VDDS18_PRTCSS
VSS_32K
PWRST
PWRCNTON
PWCTRO0
PWCTRO1
PWCTRO2
PWCTRO3
PWCTRI0
PWCTRI1
PWCTRI2
PWCTRI3
PWCTRI4
PWCTRI5
PWCTRI6
32.768KHz
Y2
C221 10pF
C220 10pF
R259 NO-POP
R268 0
R198 0
R462 0
R473 10k
R466 0
R486 10K
R478 0
R480 0
R243 10K
C195 0.1uF
U39 SN74LVC1G07
R248 10K
R247 10K
R246 10K
R245 10K
R244 10K
R483 0
R485 NO-POP
R484 10K
J28 HEADER 2
JP2 HEADER 2
TP66 TEST POINT
SW2 PUSHBUTTON SW
U13 U-74AVC8T245
C184 0.1uF
C185 0.1uF
C196 0.1uF
C211 0.1uF
C204 0.001uF
C205 0.1uF
C190 1.0uF
C191 2.2uF
R240 0.02
R241 0.02
R273 0
R274 0
R235 0
R250 10K
TP19
TP18
1V8_BB_UP
1V2_BB_UP
CPU_1V8_BB_UP
VCC_3V3
44 ALT_POWERUP_RESET
47 TPS65510_XRESET
47 TPS65510_CS
DSP_PWCTR_OUT0 10
PWCTR_OUT0 21
MSP430_PWCTR_OUT1 44
PWCTR_OUT1 48,51,52
PWCTR_OUT2
PWCTR_OUT3
PWCTR_IO1
PWCTR_IO2
PWCTR_IO3
PWCTR_IO4
PWCTR_IO5
PWCTR_IO6
3V3_PWCTR_OUT2 21
3V3_PWCTR_OUT3 21
3V3_PWCTR_IO1 21
3V3_PWCTR_IO2 21
3V3_PWCTR_IO3 21
3V3_PWCTR_IO4 21
3V3_PWCTR_IO5 21
3V3_PWCTR_IO6 21


SPECTRUM DIGITAL INCORPORATED
Title: DM365 Evaluation Module
Page Contents: DM365 POWER
Size:B
DWG NO 510842-0001
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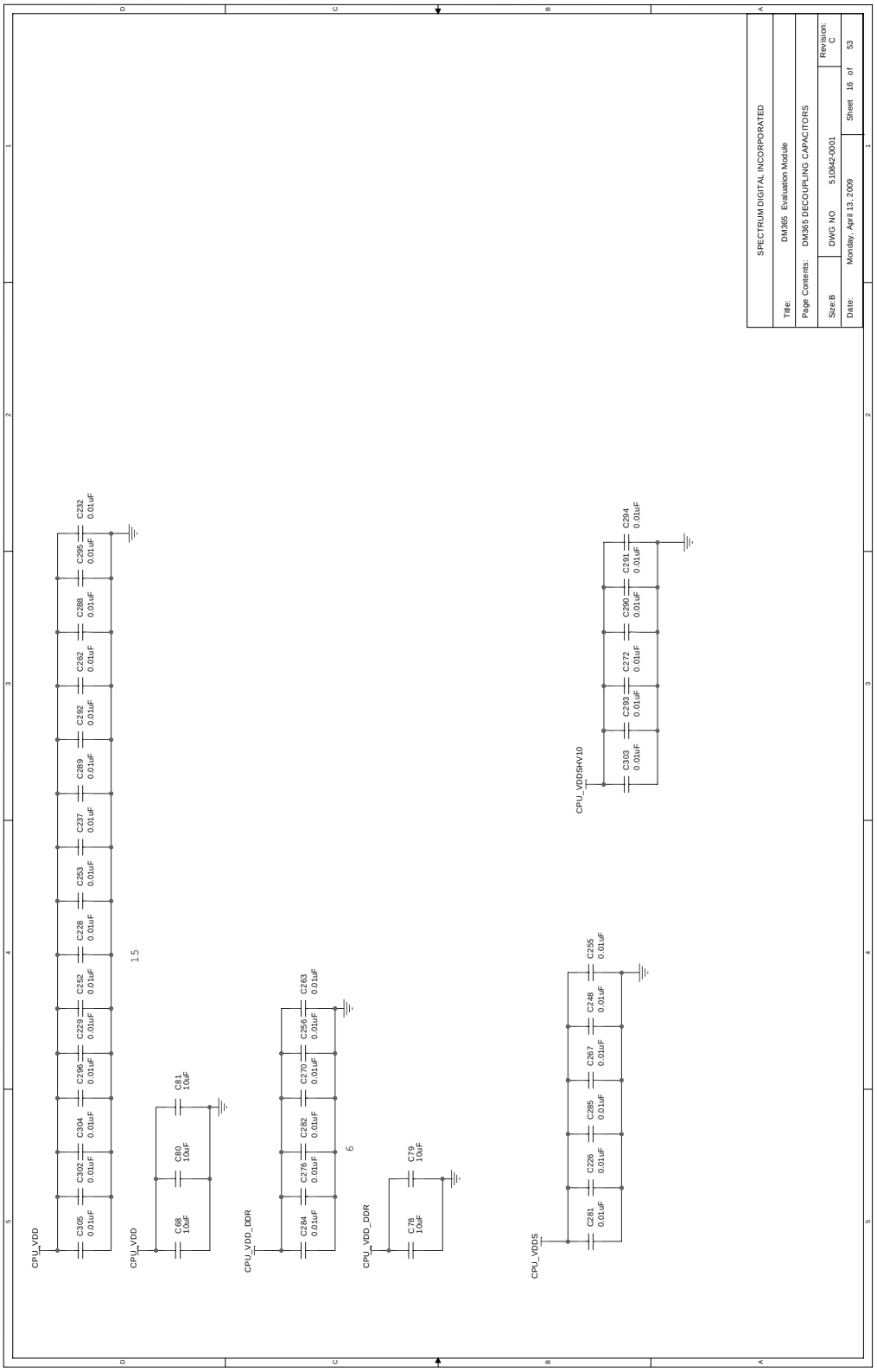
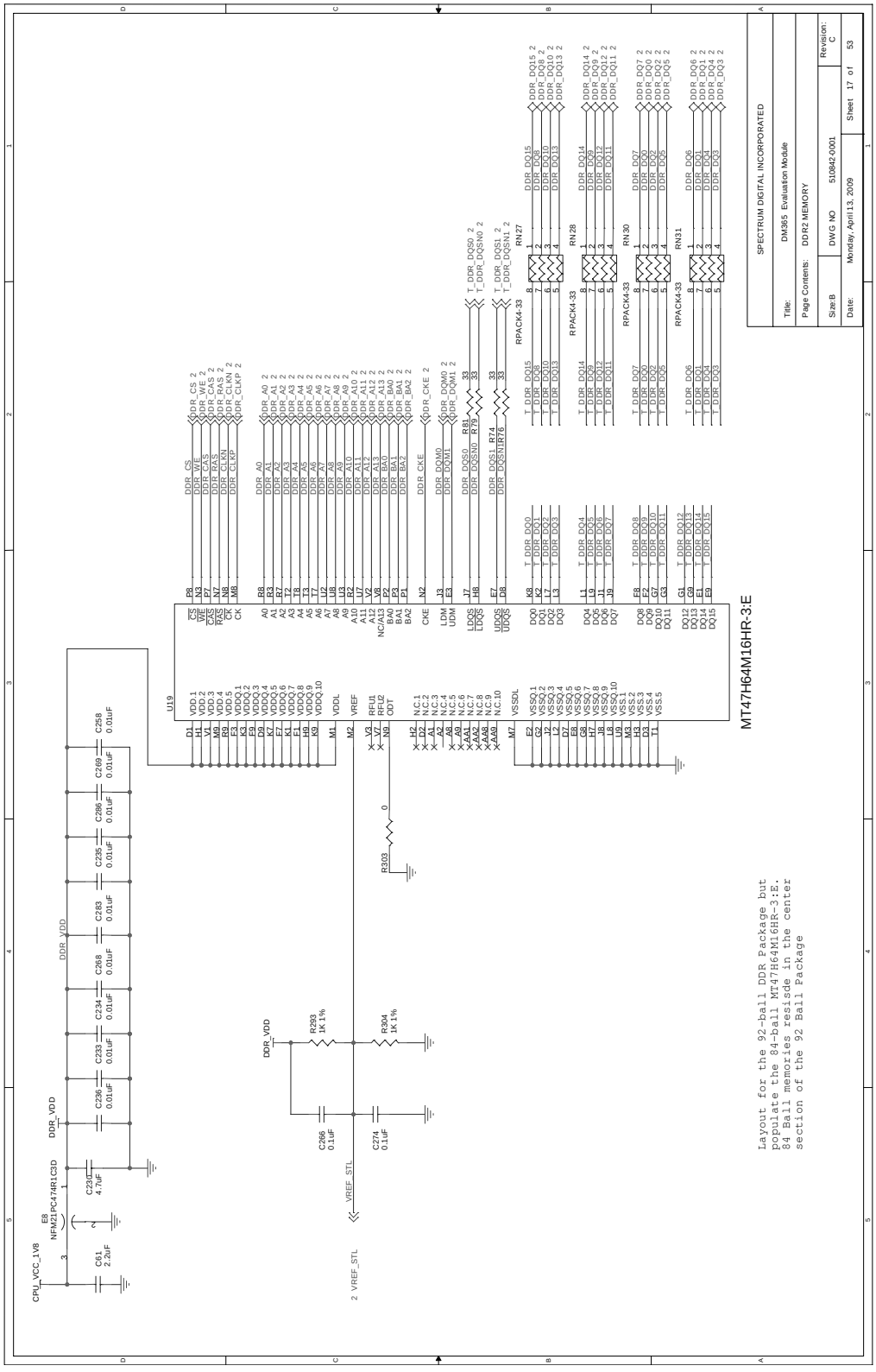
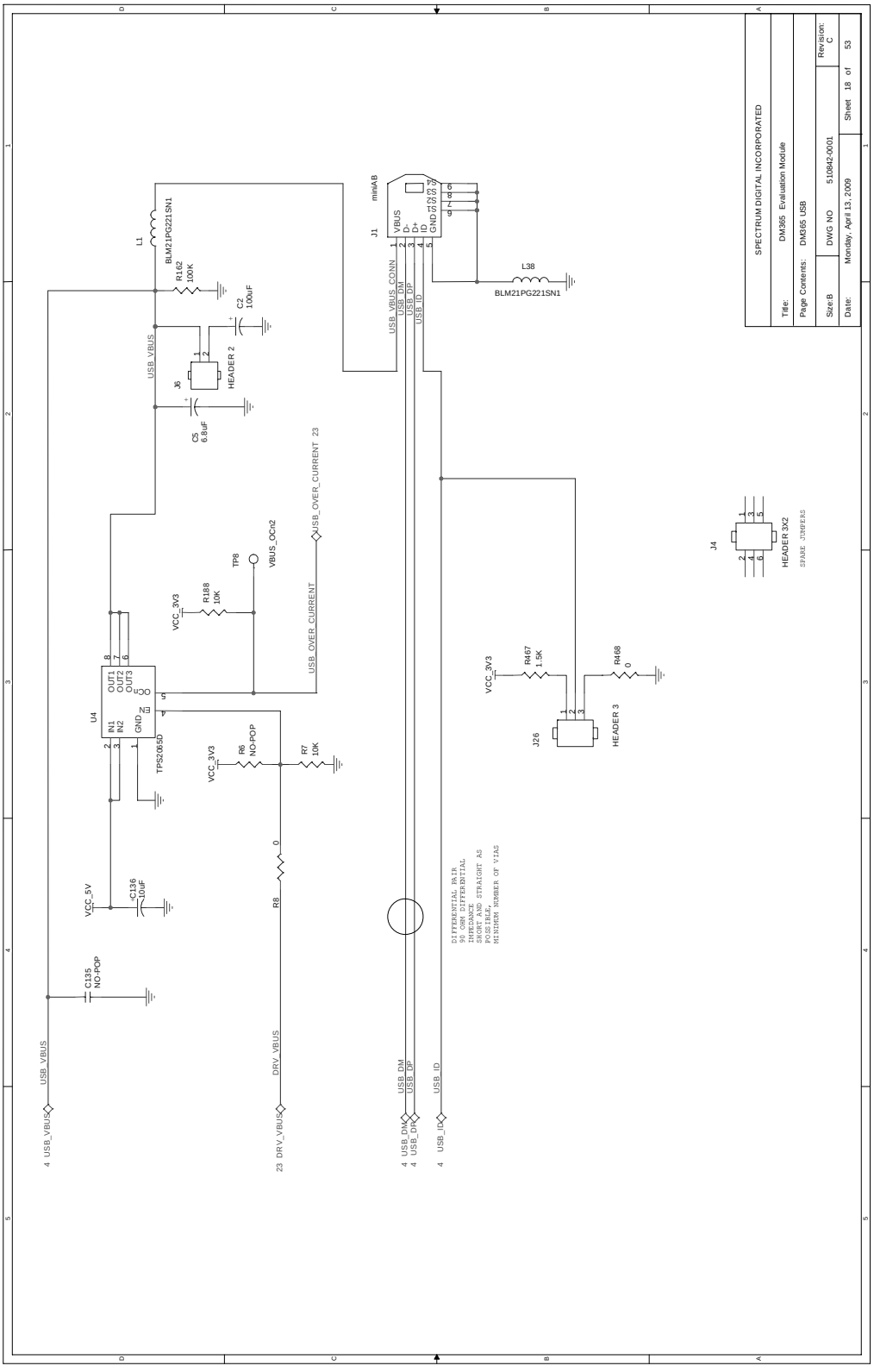
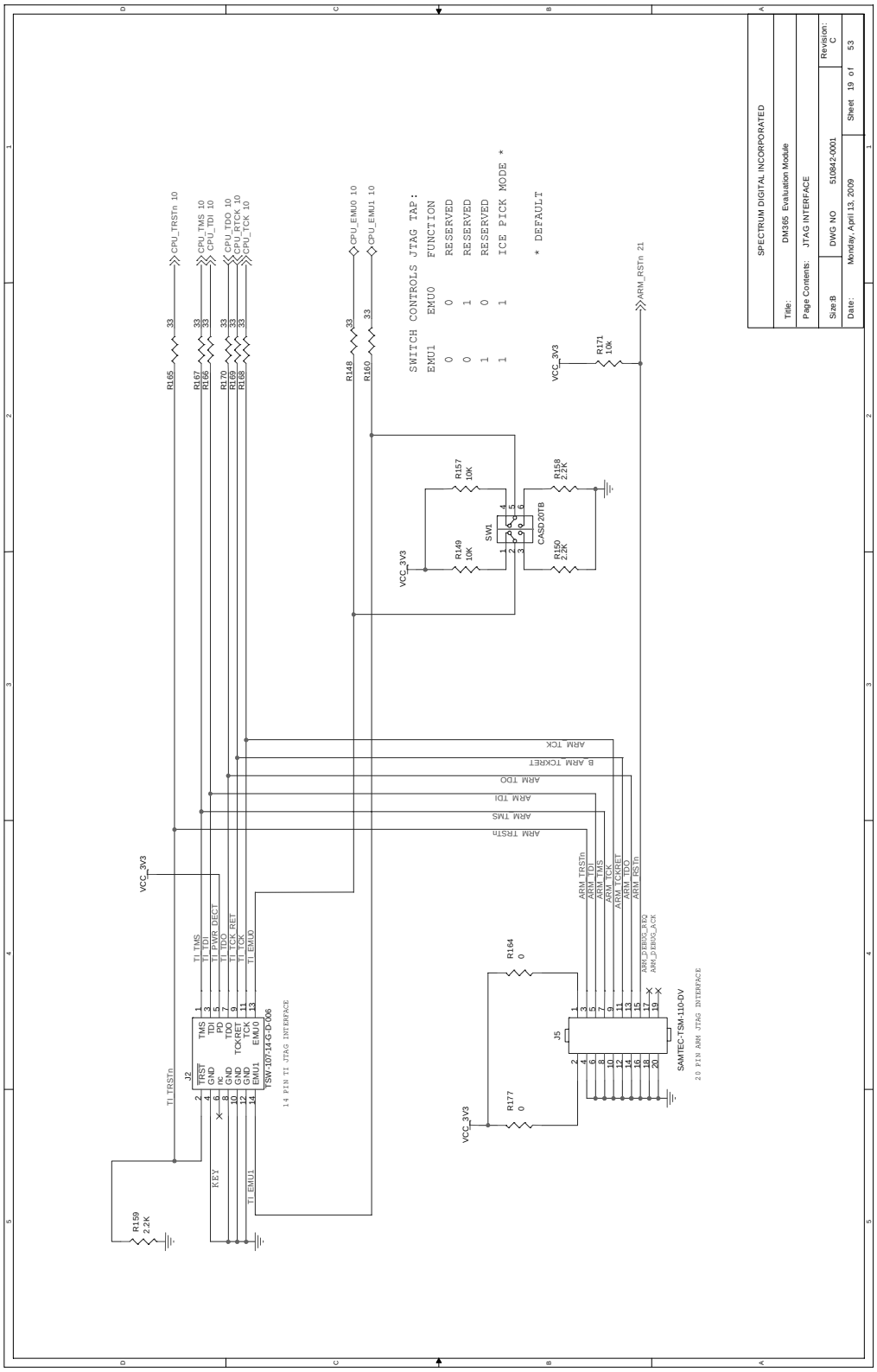
Date: Monday, April 13, 2009
Sheet 15 of 53
U18-12
TMS320DM365
U18-15
TMS320DM365
TP30 TEST POINT
TP24 TEST POINT
TP27 TEST POINT
R529 0
RSV0(NC)
RSV1(NC)
RSV2(GND)


SPECTRUM DIGITAL INCORPORATED
Title: DM365 Evaluation Module
Page Contents: DM365 DECOUPLING CAPACITORS
Size:B DWG NO 510842-0001 Revision: C
Date: Monday, April 13, 2009 Sheet 16 of 53
CPU_VDD
C305 0.01uF
C302 0.01uF
C304 0.01uF
C296 0.01uF
C229 0.01uF
C252 0.01uF
C228 0.01uF
C253 0.01uF
C237 0.01uF
C289 0.01uF
C292 0.01uF
C262 0.01uF
C288 0.01uF
C295 0.01uF
C232 0.01uF
15
CPU_VDD
C68 10uF
C80 10uF
C81 10uF
CPU_VDD_DDR
C284 0.01uF
C276 0.01uF
C282 0.01uF
C270 0.01uF
C258 0.01uF
C263 0.01uF
9
CPU_VDD_DDR
C78 10uF
C79 10uF
CPU_VDDS
C281 0.01uF
C226 0.01uF
C285 0.01uF
C267 0.01uF
C248 0.01uF
C255 0.01uF
CPU_VDDSHV10
C303 0.01uF
C293 0.01uF
C272 0.01uF
C290 0.01uF
C291 0.01uF
C294 0.01uF


SPECTRUM DIGITAL INCORPORATED
Title: DM365 Evaluation Module
Page Contents: DDR2 MEMORY
Size: B
DWG NO 510842-0001
Revision: C
Date: Monday, April 13, 2009
Sheet 17 of 53
MT47H64M16HR-3:E
U19
RPACK4-33
RN27
RN28
RN30
RN31
Layout for the 92-ball DDR Package but populate the 84-ball MT47H64M16HR-3:E. 84 Ball memories reside in the center section of the 92 Ball Package


SPECTRUM DIGITAL INCORPORATED
Title: DM365 Evaluation Module
Page Contents: DM365 USB
Size: B
DWG NO 510842-0001
Revision: C
Date: Monday, April 13, 2009
Sheet 18 of 53
L1
BLM21PG221SN1
R162
100K
C2
100uF
HEADER 2
J6
C5
6.8uF
USB_VBUS
J1
miniAB
VBUS
D-
D+
ID
GND
USB_VBUS_CONN
USB_DM
USB_DP
USB_ID
L38
BLM21PG221SN1
U4
TPS2065D
OUT1
OUT2
OUT3
IN1
IN2
GND
VCC_3V3
R188
10K
TP8
VBUS_OCnt2
USB_OVER_CURRENT
USB_OVER_CURRENT 23
R6
NO-POP
R7
10K
R8
0
VCC_5V
C136
10uF
C135
NO-POP
DRV_VBUS
USB_VBUS
USB_DM
USB_DP
USB_ID
4 USB_VBUS
23 DRV_VBUS
4 USB_DM
4 USB_DP
4 USB_ID
DIFFERENTIAL PAIR
90 OHM DIFFERNTIAL
IMPEDANCE
ROUTE AS STRAIGHT AS
POSSIBLE,
MINIMUM NUMBER OF VIAS
J4
HEADER 3X2
SPARE JUMPERS
R467
1.5K
R468
0
J26
HEADER 3


SPECTRUM DIGITAL INCORPORATED
Title: DM365 Evaluation Module
Page Contents: JTAG INTERFACE
Size:B
DWG NO 510842-0001
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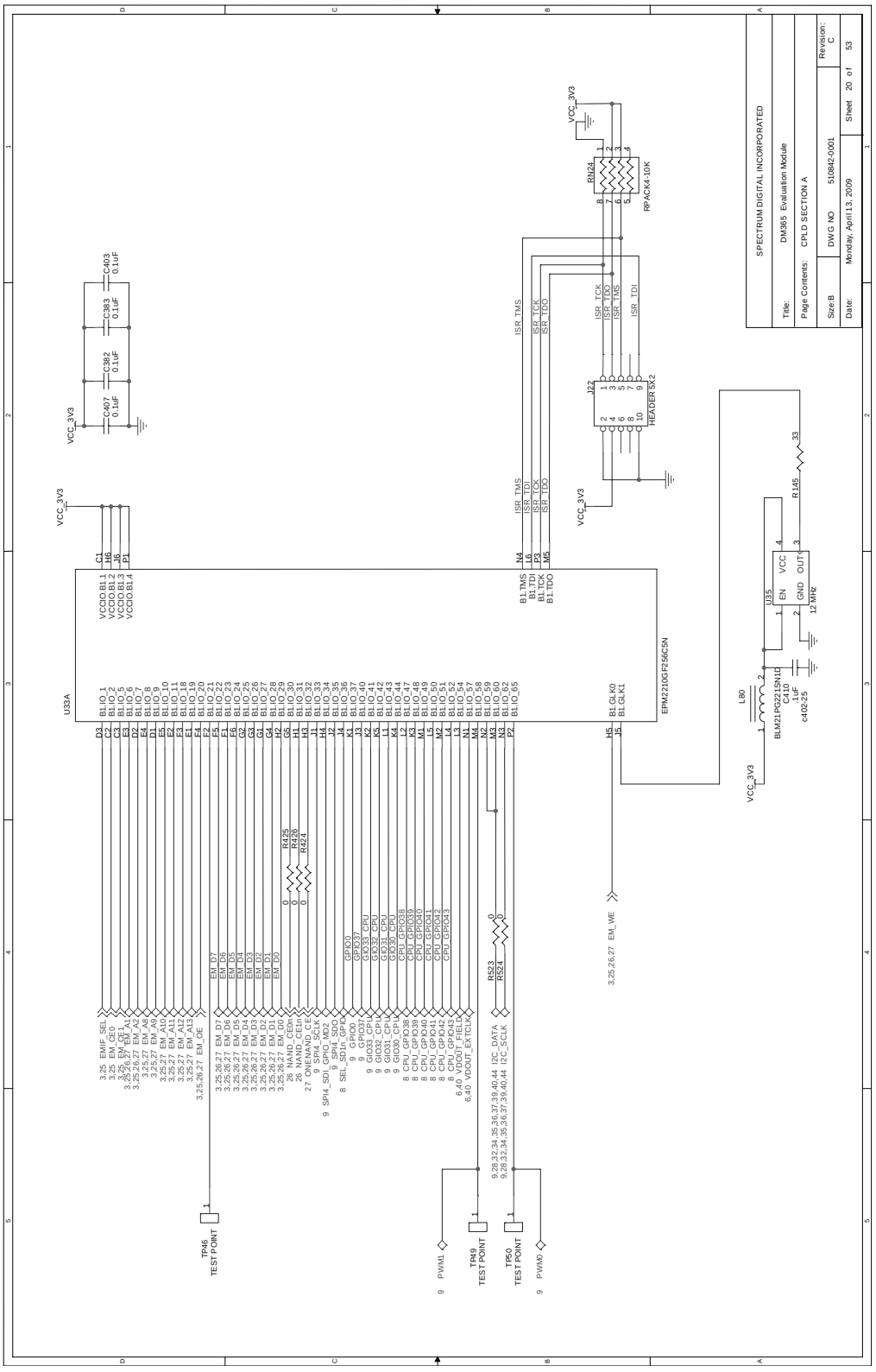
Sheet 19 of 53
SWITCH CONTROLS JTAG TAP:
EMU1 EMU0 FUNCTION
0 0 RESERVED
0 1 RESERVED
1 0 RESERVED
1 1 ICE PICK MODE *
* DEFAULT
CPU_TRSTn 10
CPU_TMS 10
CPU_TDI 10
CPU_TDO 10
CPU_RTCK 10
CPU_TCK 10
CPU_EMU0 10
CPU_EMU1 10
ARM_RSTn 21
VCC_3V3
R165 33
R167 33
R166 33
R170 33
R169 33
R168 33
R148 33
R160 33
R171 10k
R157 10K
R149 10K
R158 2.2K
R150 2.2K
SW1
CASD-207TB
R159 2.2K
R164 0
R177 0
J2
TSW-107-14-G-D-006
14 PIN TI JTAG INTERFACE
J5
SAMTEC-TSM-110-DV
20 PIN ARM JTAG INTERFACE
TI_TRSTn
TI_TMS
TI_TDI
TI_POWER_DECT
TI_TDO
TI_TCK_RET
TI_TCK
TI_EMU0
TI_EMU1
KEY
ARM_TRSTn
ARM_TDI
ARM_TMS
ARM_TCK
ARM_TCKRET
ARM_TDO
ARM_RSTn
ARM_D_EBUG_REQ
ARM_D_EBUG_ACK
ARM_TCK
B_ARM_TCKRET
ARM_TDO
ARM_TDI
ARM_TMS
ARM_TRSTn


SPECTRUM DIGITAL INCORPORATED
Title: DM365 Evaluation Module
Page Contents: CPLD SECTION A
Size:B
DWG NO 510842-0001
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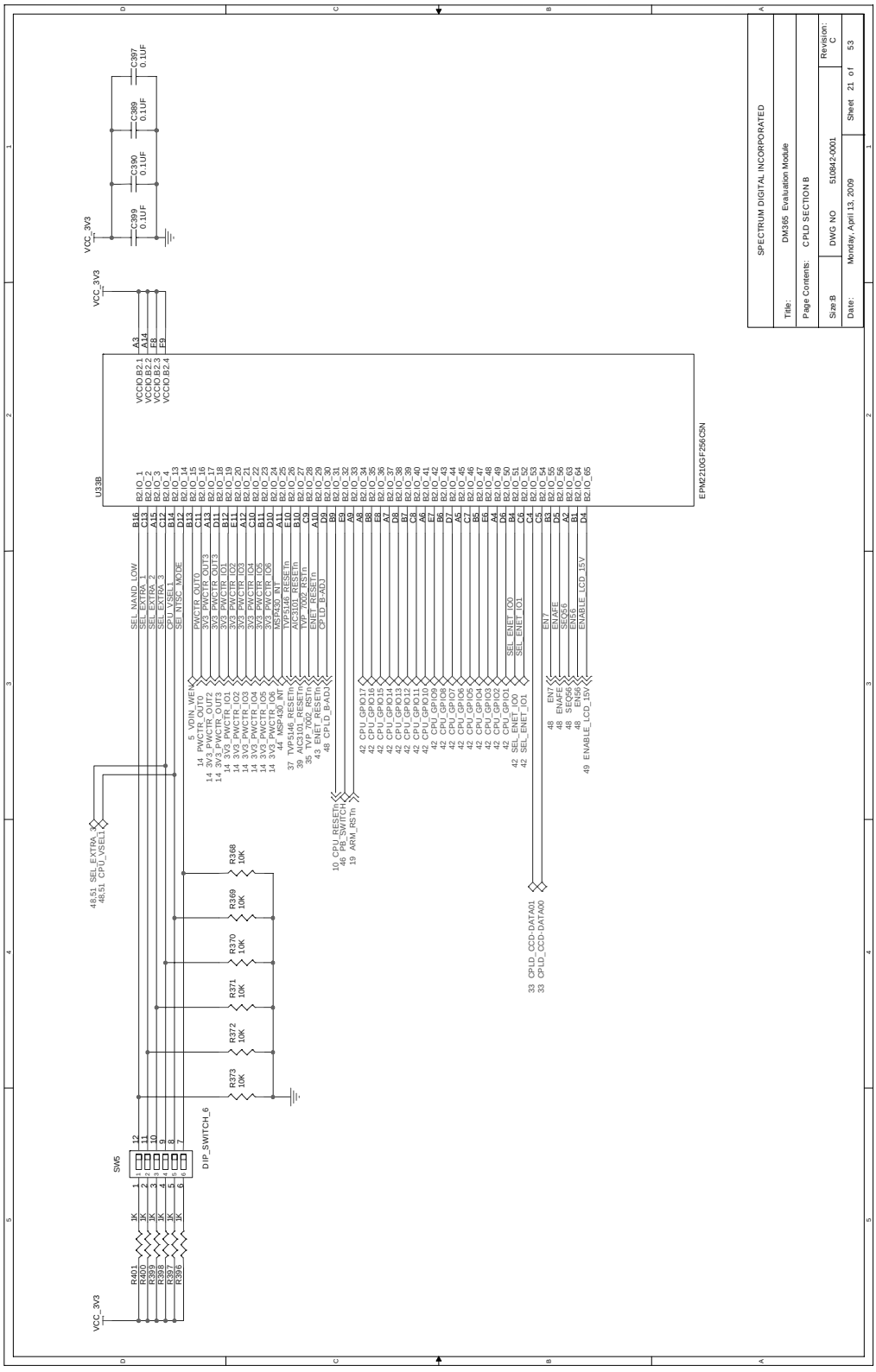
Date: Monday, April 13, 2009
Sheet 20 of 53
U33A
EPM2210GF256C5N
U35
12 MHz
L80
BLM21PG221SN1D
RN24
RPACK4-10K
J22
HEADER 5X2
TP46
TP49
TP50
TEST POINT
VCC_3V3
ISR_TMS
ISR_TDI
ISR_TCK
ISR_TDO
EM_WE
I2C_DATA
I2C_SCLK
PWM1
PWM0


SPECTRUM DIGITAL INCORPORATED
Title: DM365 Evaluation Module
Page Contents: CPLD SECTION B
Size:B
DWG NO 510842-0001
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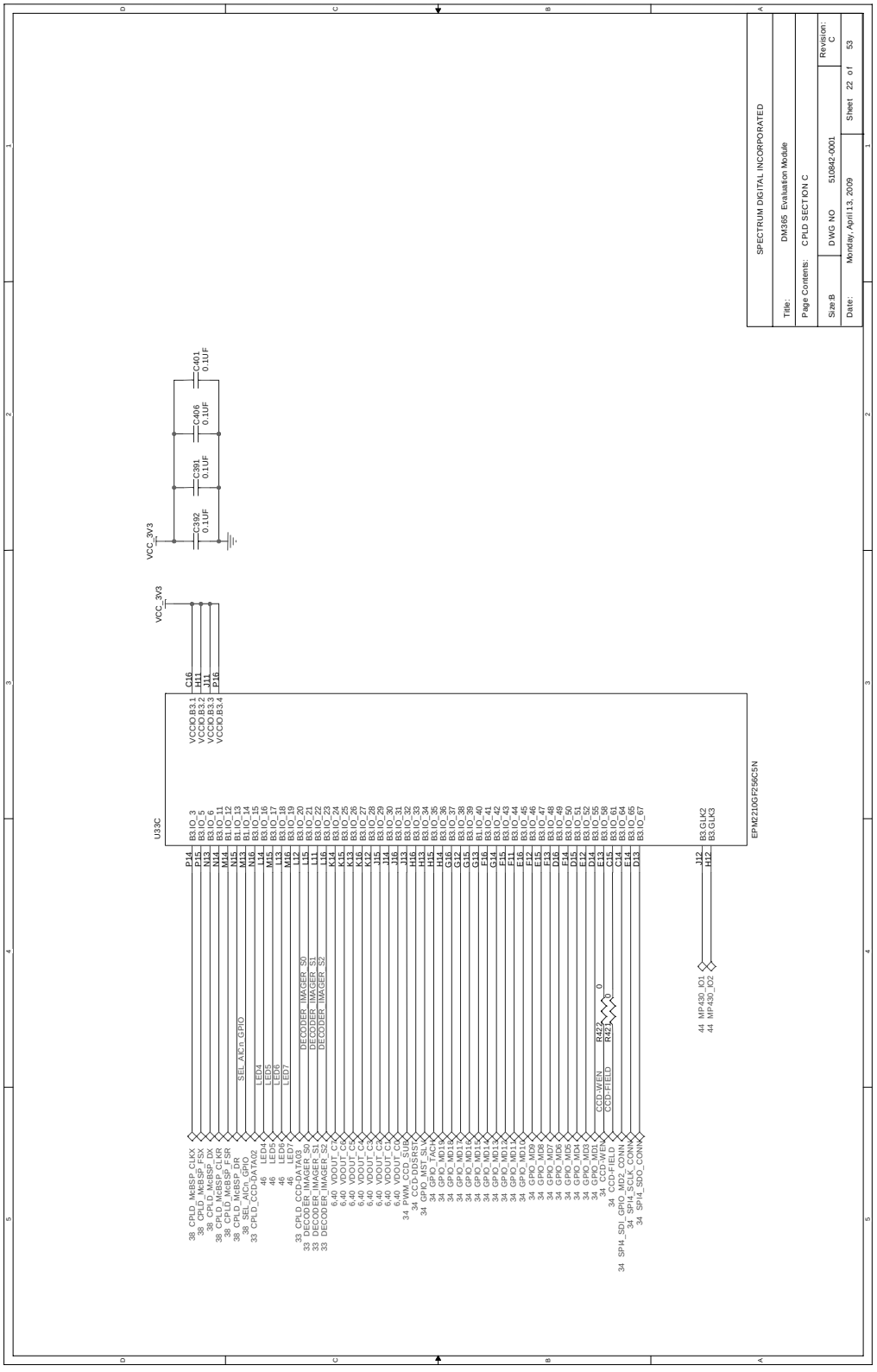
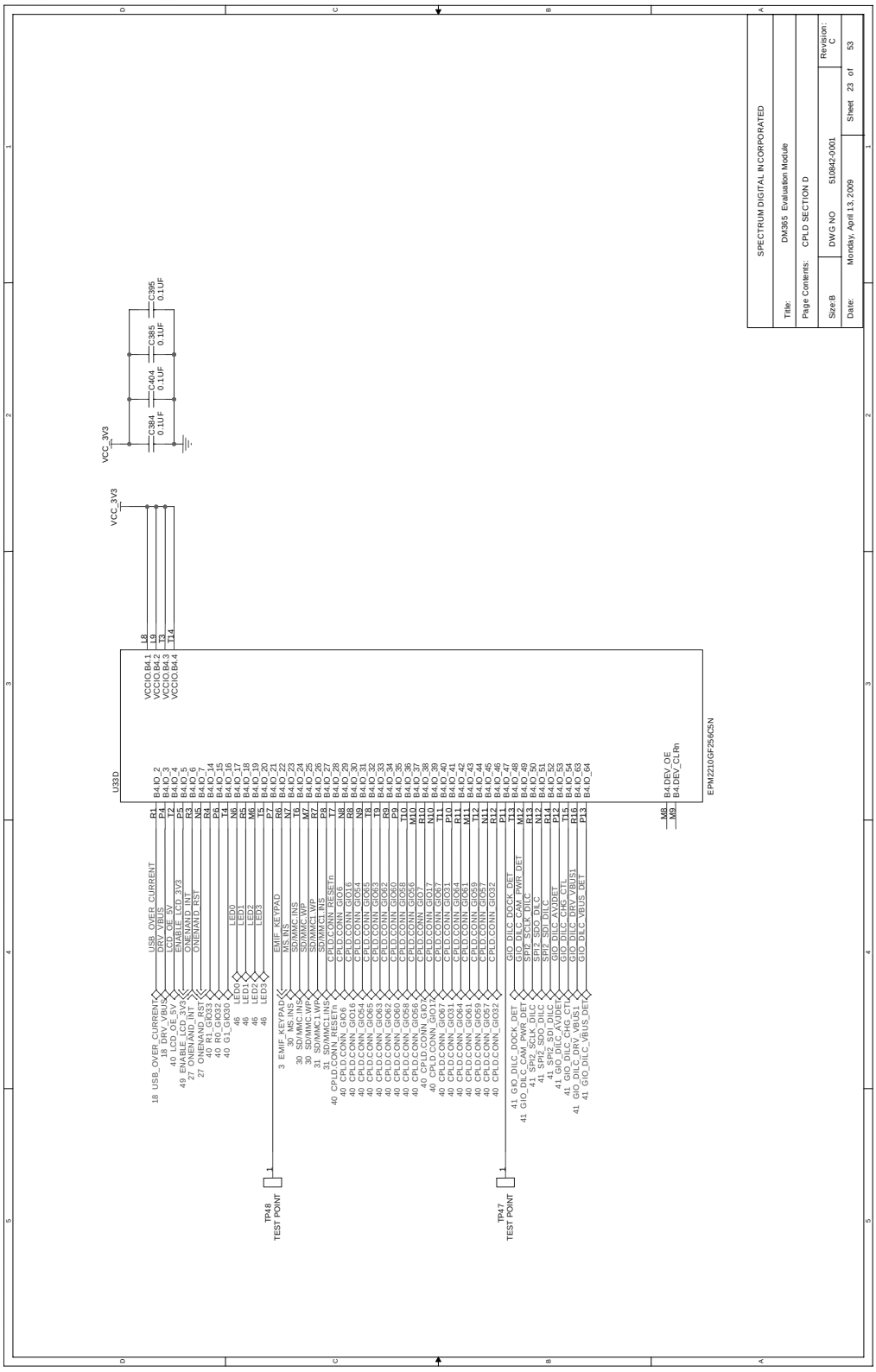
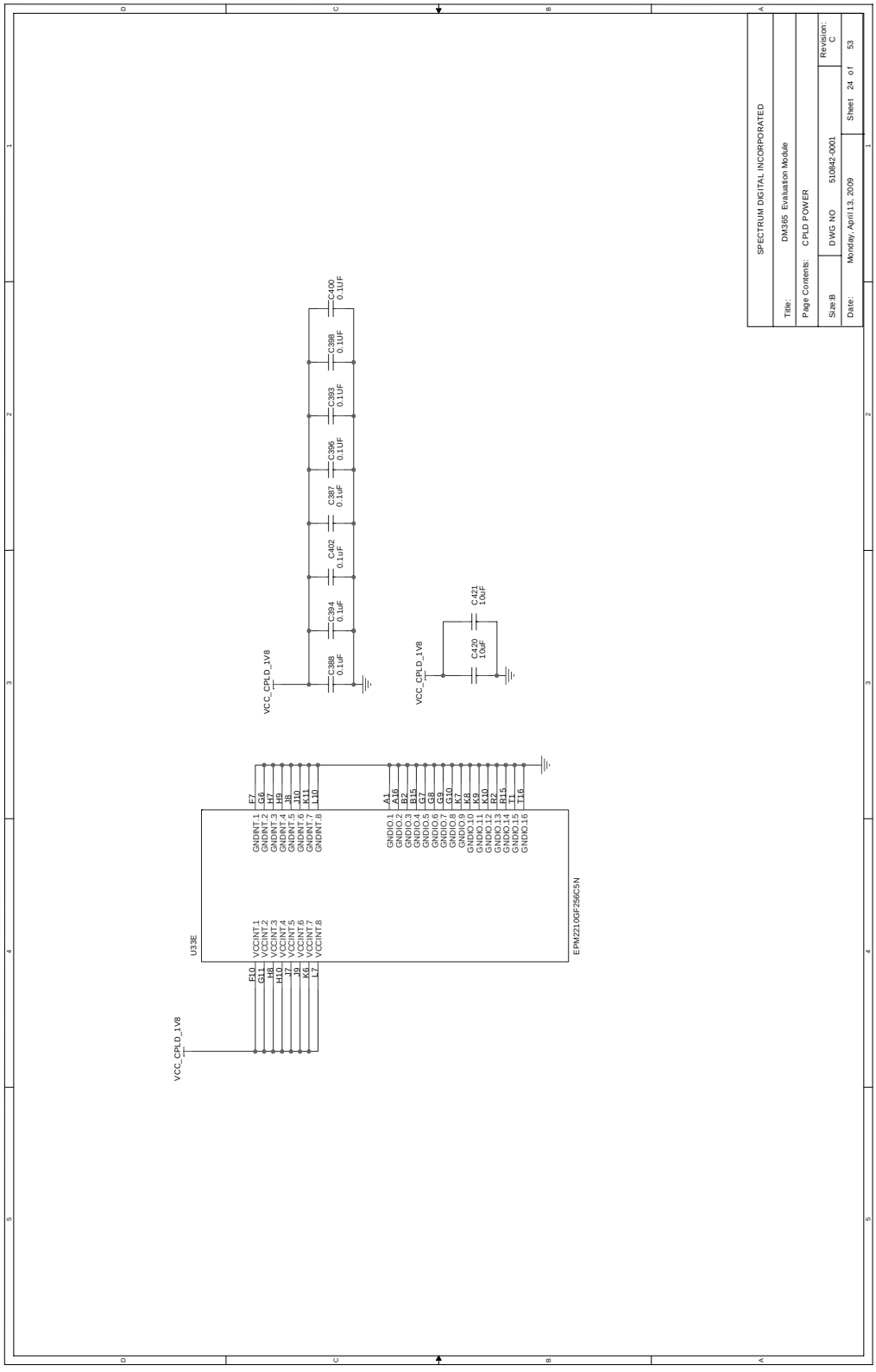
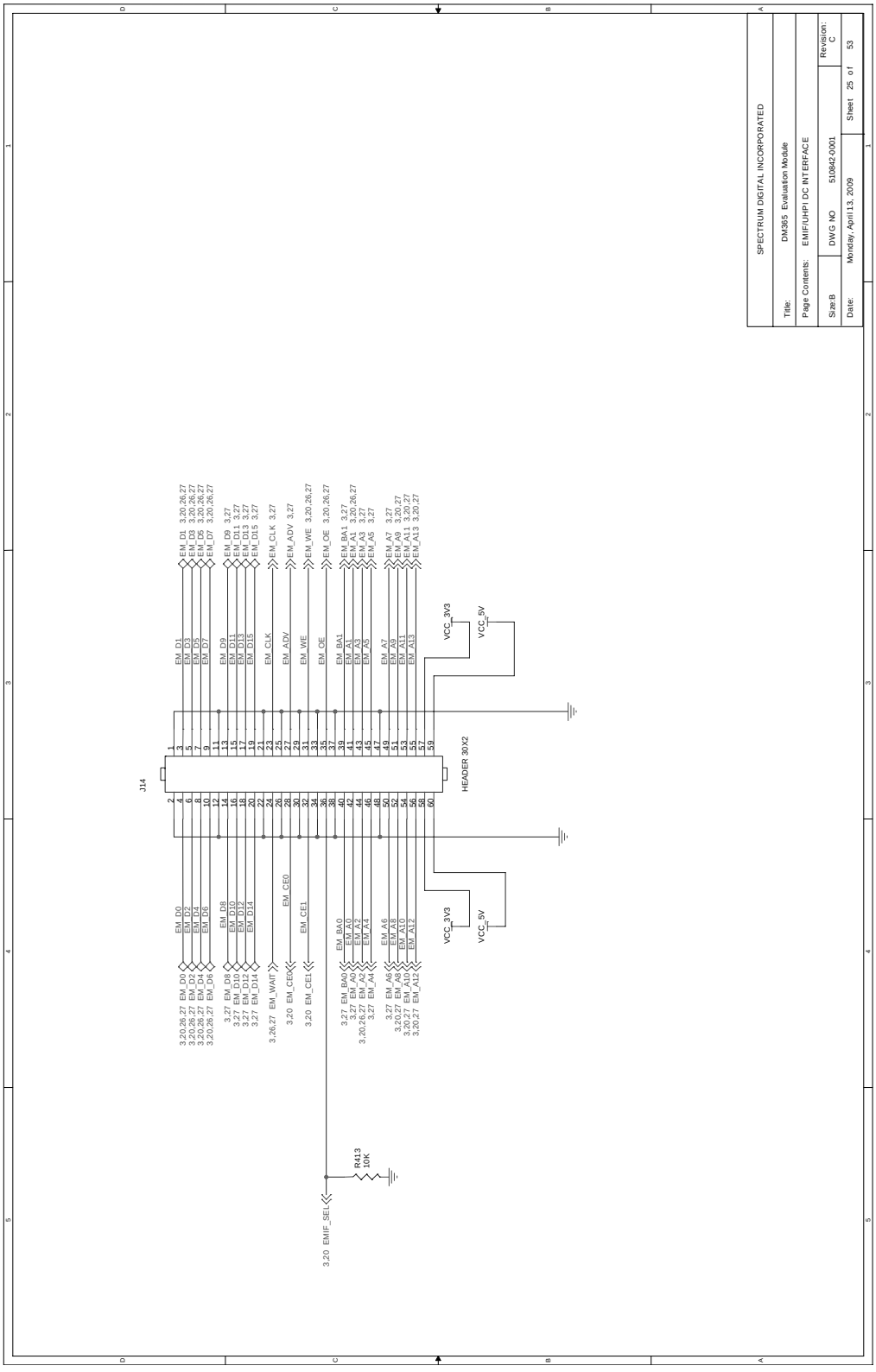
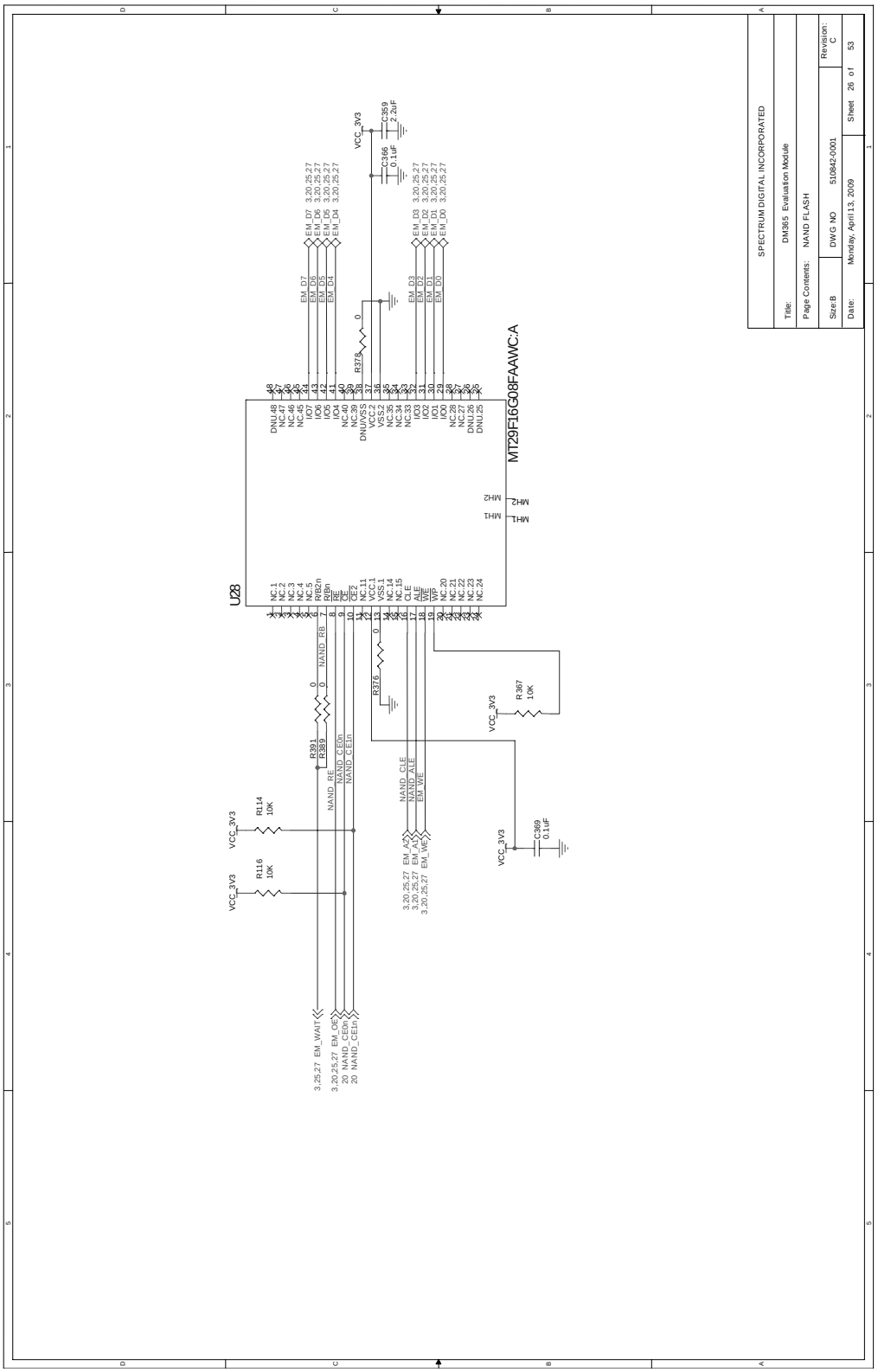
Date: Monday, April 13, 2009
Sheet 21 of 53
U33B
EPM2210GF256C5N
SW5
DIP_SWITCH_6
VCC_3V3
C397 0.1UF
C389 0.1UF
C390 0.1UF
C399 0.1UF
R401 1K
R400 1K
R399 1K
R398 1K
R397 1K
R396 1K
R368 10K
R369 10K
R370 10K
R371 10K
R372 10K
R373 10K
SEL_NAND_LOW
SEL_EXTRA_1
SEL_EXTRA_2
SEL_EXTRA_3
CPU_VSEL1
SEL_NTSC_MODE
PWCTR_OUT0
3V3_PWCTR_OUT3
3V3_PWCTR_OUT2
3V3_PWCTR_IO1
3V3_PWCTR_IO2
3V3_PWCTR_IO3
3V3_PWCTR_IO4
3V3_PWCTR_IO5
3V3_PWCTR_IO6
MSP430_INT
TVP5146_RESETn
AIC3101_RESETn
TVP 7002_RSTn
ENET_RESETn
CPLD_BAD1
CPU_GPIO17
CPU_GPIO16
CPU_GPIO15
CPU_GPIO14
CPU_GPIO13
CPU_GPIO12
CPU_GPIO11
CPU_GPIO10
CPU_GPIO9
CPU_GPIO8
CPU_GPIO7
CPU_GPIO6
CPU_GPIO5
CPU_GPIO4
CPU_GPIO3
CPU_GPIO2
CPU_GPIO1
SEL_ENET_IO0
SEL_ENET_IO1
EN7
ENAFE
SEQ96
EN36
ENABLE_LCD_15V
CPLD_CCD-DATA01
CPLD_CCD-DATA00
CPU_RESETn
PB_SWITCH
ARM_RSTn

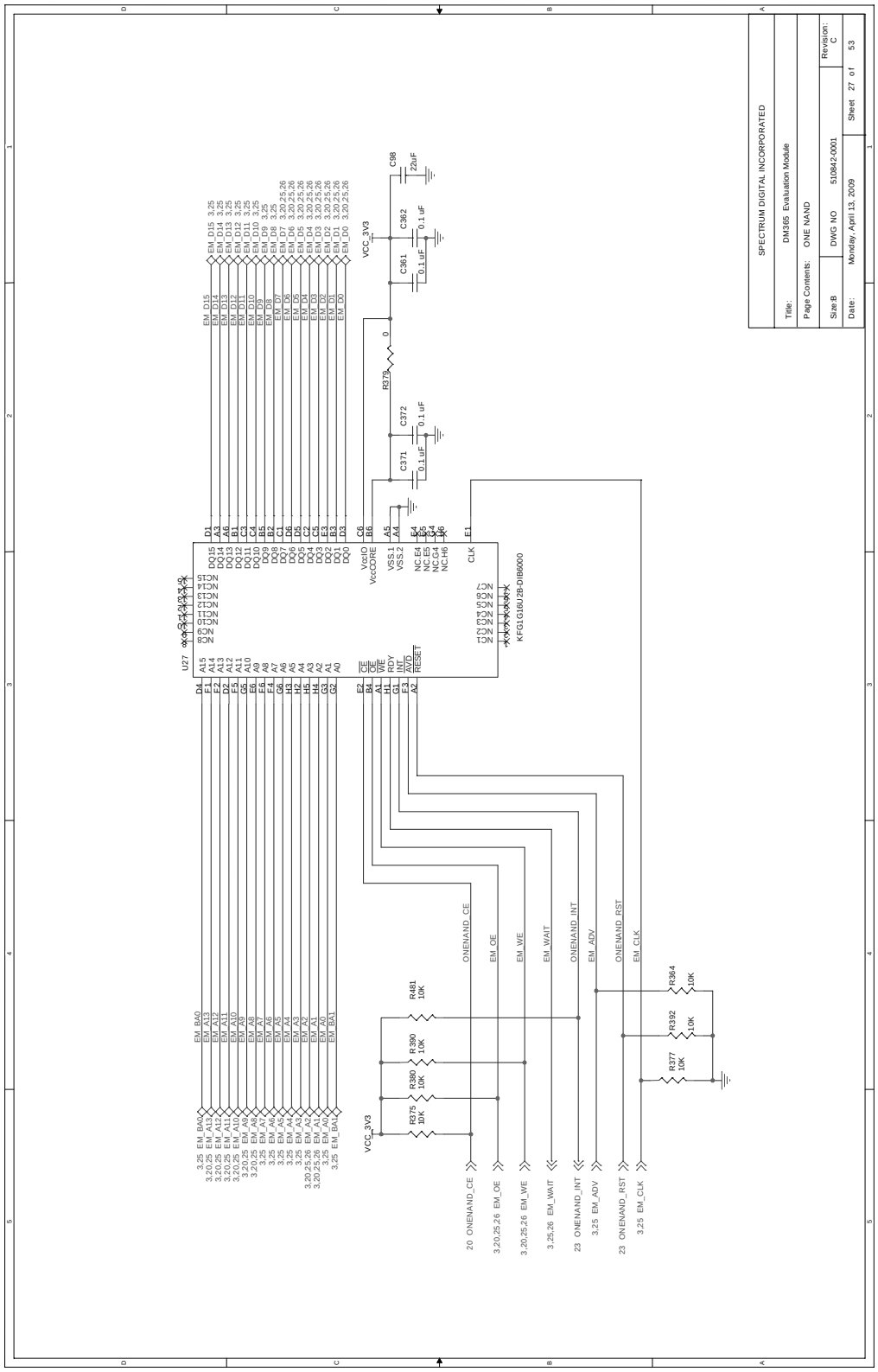

SPECTRUM DIGITAL INCORPORATED
Title: DM365 Evaluation Module
Page Contents: CPLD SECTION C
Size:B
DWG NO 510842-0001
Revision: C
Date: Monday, April 13, 2009
Sheet 22 of 53
U33C
EPM2210GF256C5N
VCC_3V3
C392 0.1UF
C391 0.1UF
C406 0.1UF
C401 0.1UF
C16
H11
J11
P16
VCCIO B3.1
VCCIO B3.2
VCCIO B3.3
VCCIO B3.4
R422 0
R423 0
SEL_AICn_GPIO
LED4
LED5
LED6
LED7
DECODER_IMAGER_S0
DECODER_IMAGER_S1
DECODER_IMAGER_S2
CCD-WEN
CCD-FIELD
MP430_IO1
MP430_IO2
B3_CLK2
B3_CLK3

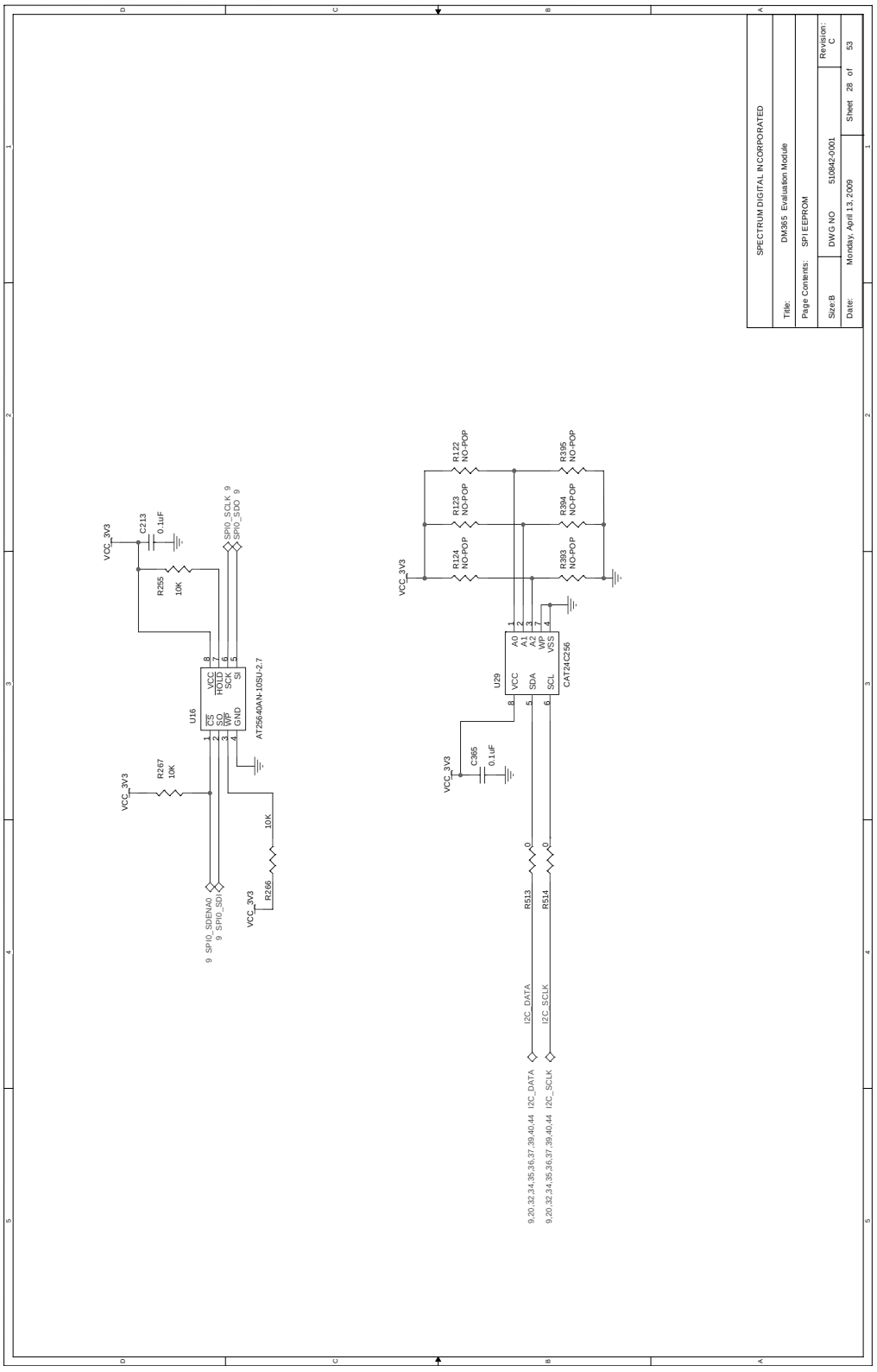

SPECTRUM DIGITAL INCORPORATED
Title: DM365 Evaluation Module
Page Contents: CPLD SECTION D
Size:B
DWG NO 510842-0001
Revision: C
Date: Monday, April 13, 2009
Sheet 23 of 53
U3D
EPM2210GF256ZSN
VCC_3V3
C394 0.1UF
C404 0.1UF
C395 0.1UF
C396 0.1UF
TP48 TEST POINT
TP47 TEST POINT

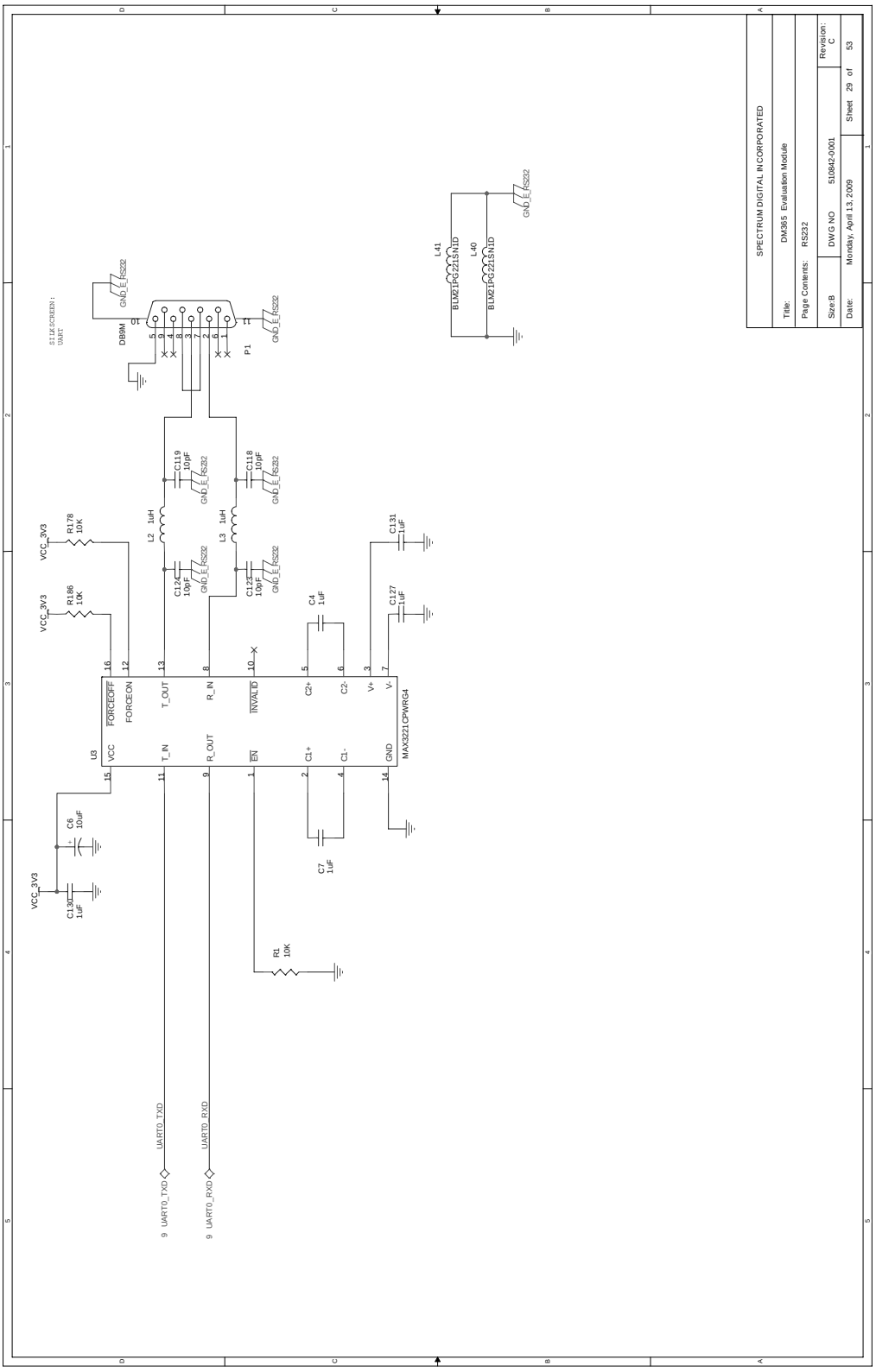

SPECTRUM DIGITAL INCORPORATED
Title: DM365 Evaluation Module
Page Contents: CPLD POWER
Size:B
DWG NO 510842-0001
Revision: C
Date: Monday, April 13, 2009
Sheet 24 of 53
C400 0.1UF
C398 0.1UF
C393 0.1UF
C396 0.1UF
C387 0.1uF
C402 0.1uF
C394 0.1uF
C388 0.1uF
C421 10uF
C420 10uF
VCC_CPLD_1V8
U33E
EPM2210GF256C5N
GNDINT.1 F7
GNDINT.2 G6
GNDINT.3 H7
GNDINT.4 H9
GNDINT.5 J8
GNDINT.6 J10
GNDINT.7 K11
GNDINT.8 L10
GNDIO.1 A1
GNDIO.2 A16
GNDIO.3 B2
GNDIO.4 B15
GNDIO.5 G7
GNDIO.6 G8
GNDIO.7 G9
GNDIO.8 G10
GNDIO.9 K7
GNDIO.10 K8
GNDIO.11 K9
GNDIO.12 K10
GNDIO.13 R2
GNDIO.14 R15
GNDIO.15 T1
GNDIO.16 T16
VCCINT.1 F10
VCCINT.2 G11
VCCINT.3 H6
VCCINT.4 H10
VCCINT.5 J7
VCCINT.6 J9
VCCINT.7 K6
VCCINT.8 L7

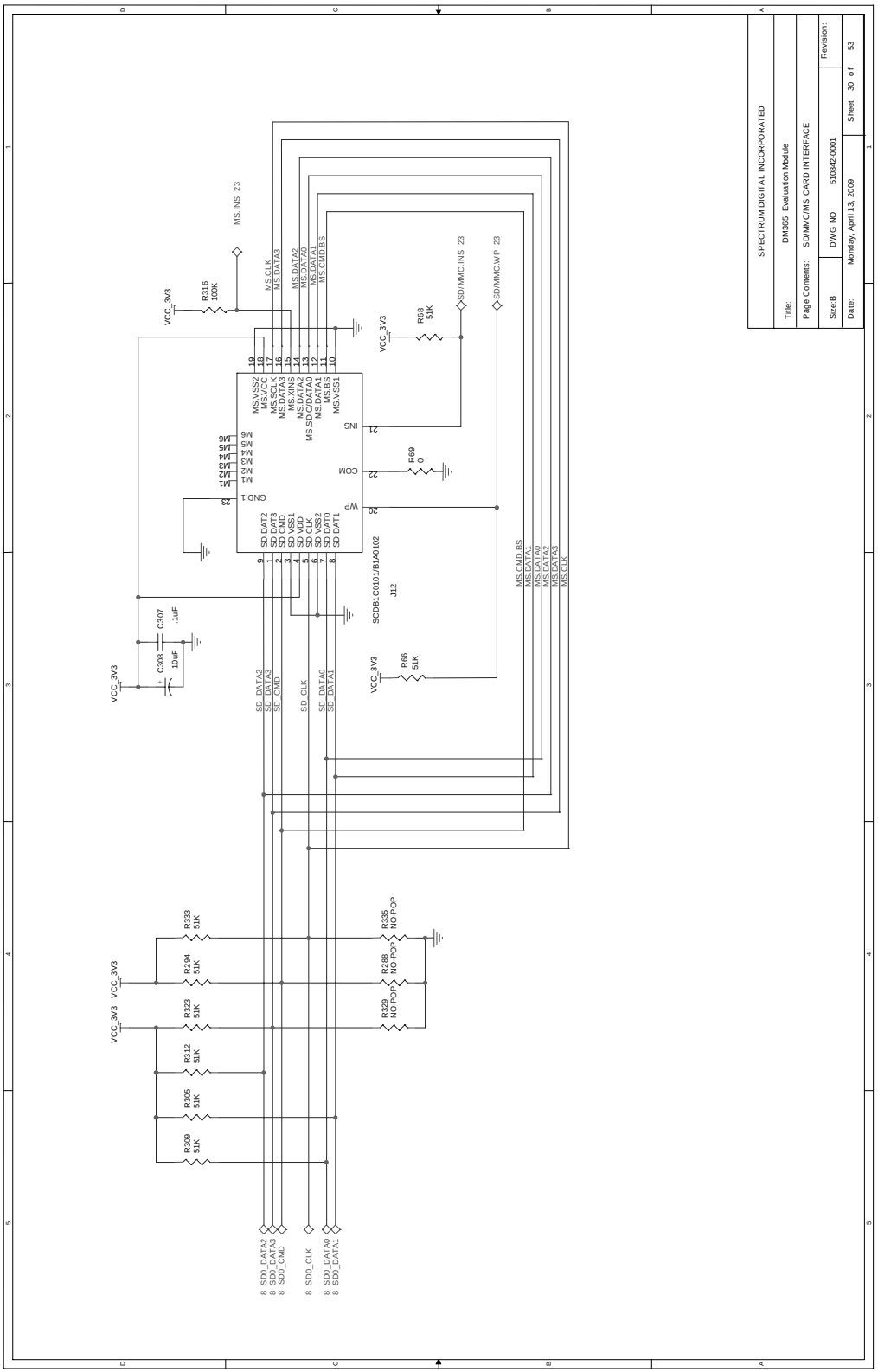

SPECTRUM DIGITAL INCORPORATED
Title: DM365 Evaluation Module
Page Contents: EMIF/UHPI DC INTERFACE
Size: B
DWG NO 510842-0001
Revision: C
Date: Monday, April 13, 2009
Sheet 25 of 53
J14
HEADER 30X2
R413
10K
VCC_3V3
VCC_5V
EM_D0
EM_D1
EM_D2
EM_D3
EM_D4
EM_D5
EM_D6
EM_D7
EM_D8
EM_D9
EM_D10
EM_D11
EM_D12
EM_D13
EM_D14
EM_D15
EM_CE0
EM_CE1
EM_WAIT
EM_CLK
EM_ADV
EM_WE
EM_OE
EM_BA0
EM_BA1
EM_A0
EM_A1
EM_A2
EM_A3
EM_A4
EM_A5
EM_A6
EM_A7
EM_A8
EM_A9
EM_A10
EM_A11
EM_A12
EM_A13
EMIF_SEL

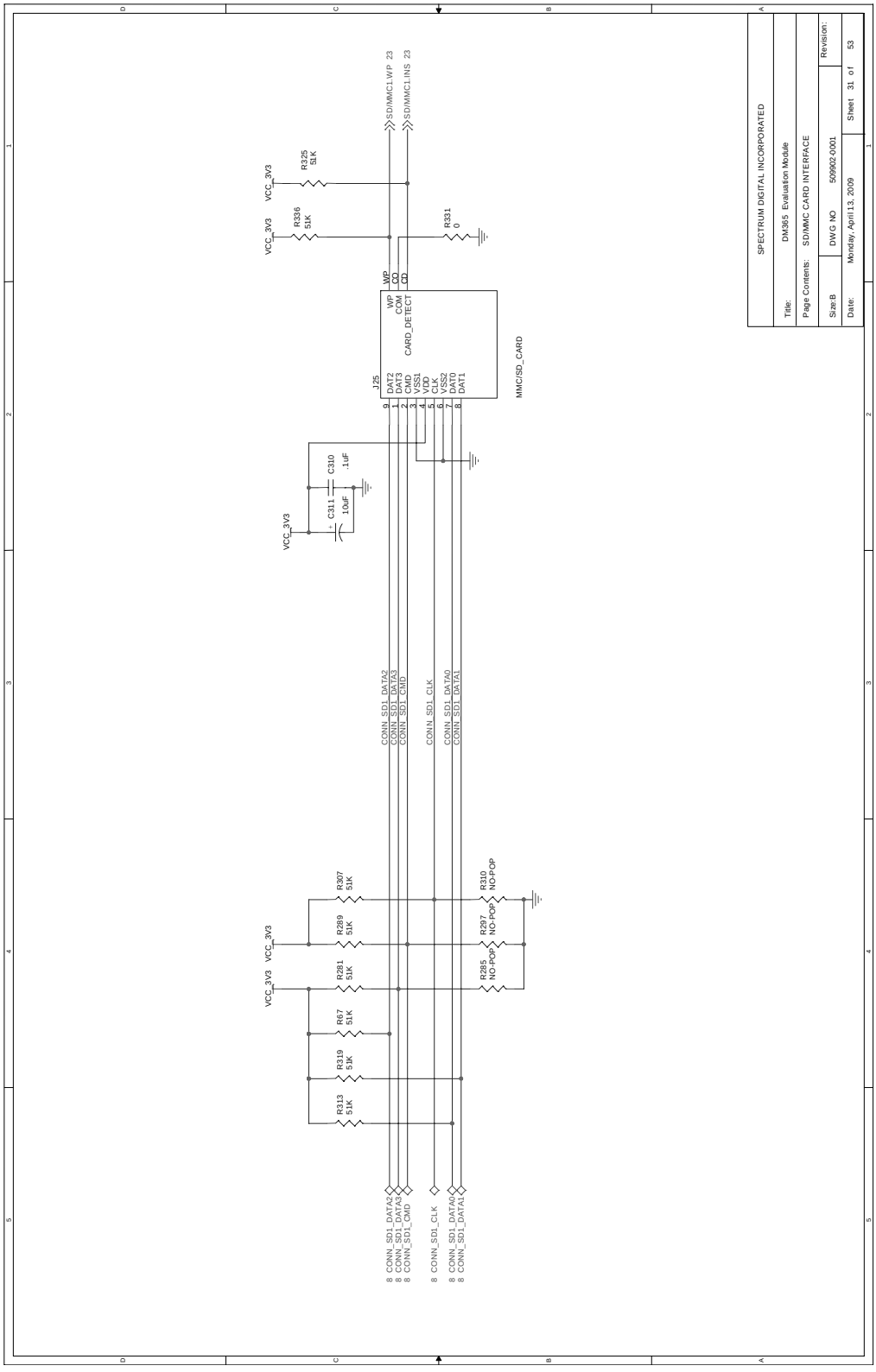

SPECTRUM DIGITAL INCORPORATED
Title: DM365 Evaluation Module
Page Contents: NAND FLASH
Size:B
DWG NO 510842-0001
Revision: C
Date: Monday, April 13, 2009
Sheet 26 of 53
U28
MT29F16G08FAAWC:A
VCC_3V3
C359 2.2uF
C366 0.1uF
R378 0
EM_D7 EM_D6 EM_D5 EM_D4
EM_D3 EM_D2 EM_D1 EM_D0
R391 0
R389 0
NAND_RB
NAND_RE
NAND_CE1n
NAND_CE0n
R376 0
NAND_CLE
NAND_ALE
EM_WE
R367 10K
R114 10K
R116 10K
C369 0.1uF
EM_WAIT
EM_OE
NAND_CE0n
NAND_CE1n
EM_A23
EM_A22
EM_WE

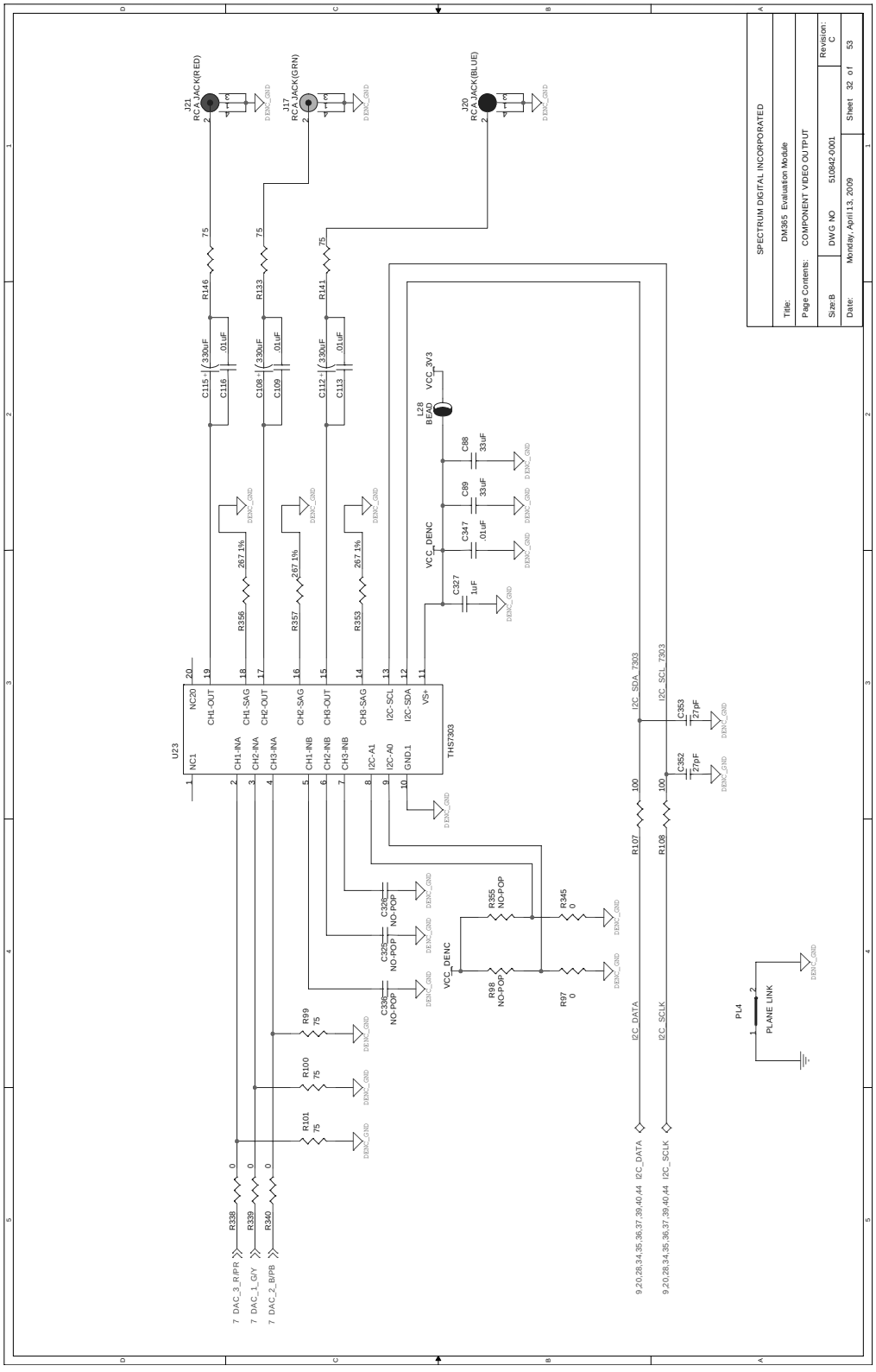

SPECTRUM DIGITAL INCORPORATED
Title: DM365 Evaluation Module
Page Contents: ONE NAND
Size:B
DWG NO 510842-0001
Revision: C
Date: Monday, April 13, 2009
Sheet 27 of 53
U27
KFG1G16U2B-DIB6000
VCC_3V3
C98 22uF
C362 0.1 uF
C361 0.1 uF
R379 0
C372 0.1 uF
C371 0.1 uF
R481 10K
R390 10K
R380 10K
R375 10K
R384 10K
R392 10K
R377 10K
ONENAND_CE
EM_OE
EM_WE
EM_WAIT
ONENAND_INT
EM_ADV
ONENAND_RST
EM_CLK

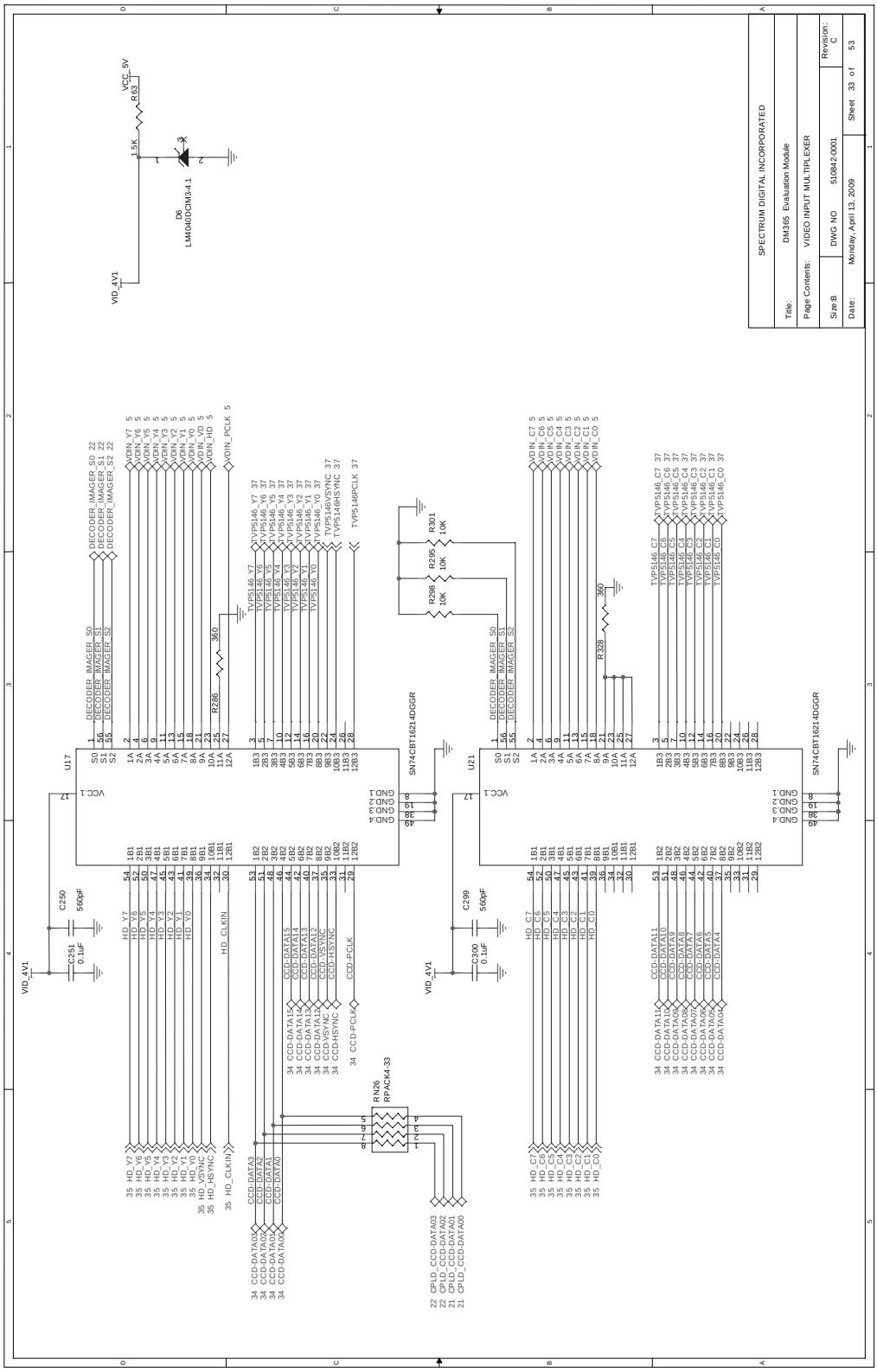

SPECTRUM DIGITAL INCORPORATED
Title: DM365 Evaluation Module
Page Contents: SPI EEPROM
Size:B
DWG NO 510842-0001
Revision: C
Date: Monday, April 13, 2009
Sheet 28 of 53
VCC_3V3
C213
0.1uF
R255
10K
SPI0_SCLK 9
SPI0_SDO 9
U16
AT25640AN-10SU-2.7
R267
10K
R266
10K
9 SPI0_SDENA0
9 SPI0_SDI
R122
NO-POP
R123
NO-POP
R124
NO-POP
R395
NO-POP
R394
NO-POP
R393
NO-POP
U29
CAT24C256
C365
0.1uF
R513
0
R514
0
I2C_DATA
I2C_SCLK
9,20,32,34,35,36,37,39,40,44 I2C_DATA
9,20,32,34,35,36,37,39,40,44 I2C_SCLK

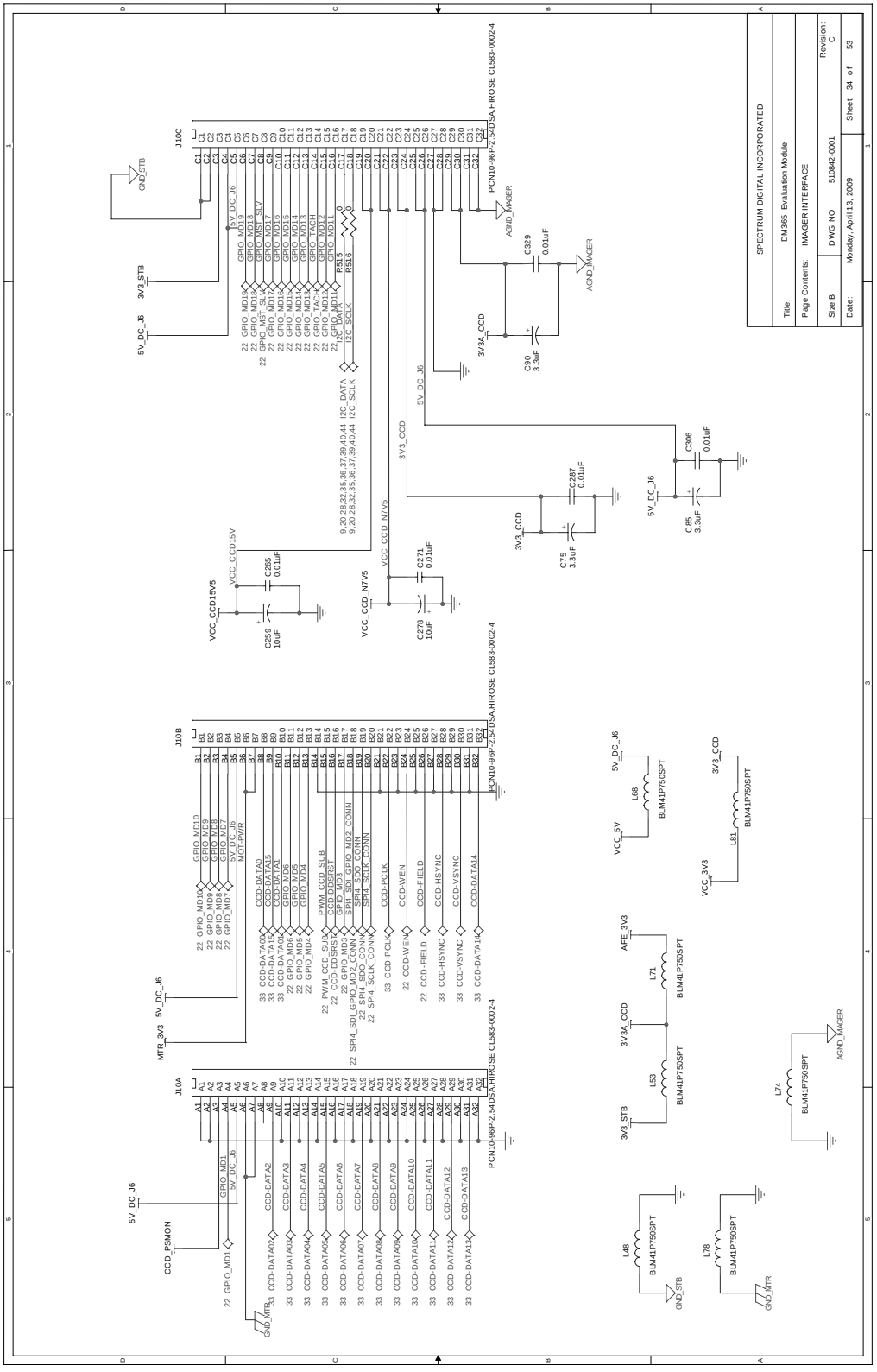

SPECTRUM DIGITAL INCORPORATED
Title: DM365 Evaluation Module
Page Contents: RS232
Size:B
DWG NO 510842-0001
Revision: C
Date: Monday, April 13, 2009
Sheet 29 of 53
U3
MAX3221CPWRG4
VCC
T_IN
R_OUT
EN
C1+
C1-
GND
FORCEOFF
FORCEON
T_OUT
R_IN
INVALID
C2+
C2-
V+
V-
DB9M
P1
L2 1uH
L3 1uH
L41
L40
BLM21PG221SN1D
C119 10pF
C118 10pF
C124 10pF
C123 10pF
C4 1uF
C131 1uF
C127 1uF
C7 1uF
C5 10uF
C130 1uF
R178 10K
R186 10K
R1 10K
VCC_3V3
GND_E_RS232
UART0_TXD
UART0_RXD
9 UART0_TXD
9 UART0_RXD

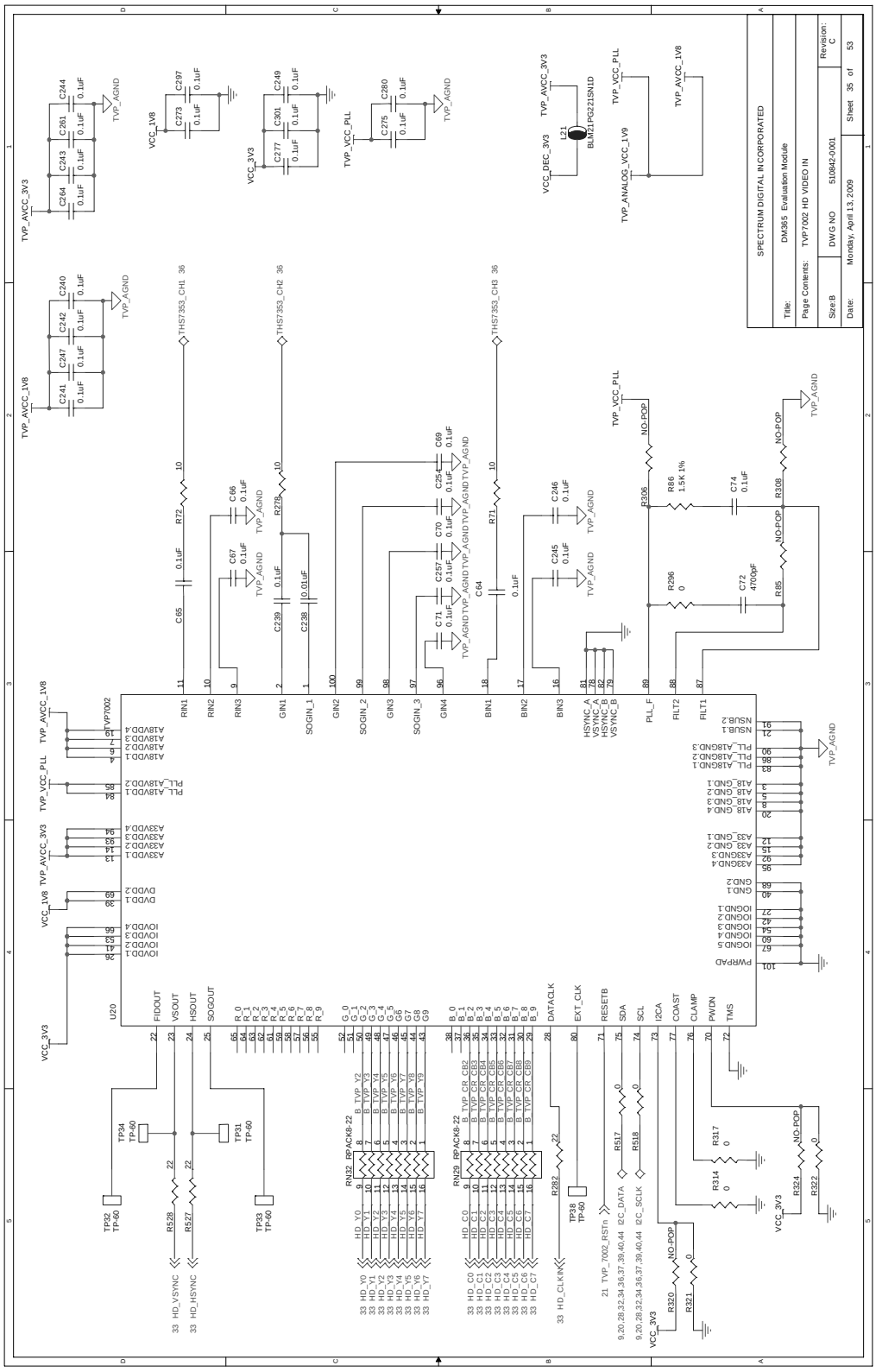

SPECTRUM DIGITAL INCORPORATED
Title: DM365 Evaluation Module
Page Contents: SD/MMC/MS CARD INTERFACE
Size:B
DWG NO 510842-0001
Revision:
Date: Monday, April 13, 2009
Sheet 30 of 53
MS.INS 23
SD/MMC.INS 23
SD/MMC.WP 23
MS_CLK
MS.DATA3
MS.DATA2
MS.DATA0
MS.DATA1
MS.CMD.BS
VCC_3V3
R316 100K
R68 51K
R69 0
R66 51K
C307 .1uF
C308 10uF
J12
SCDB1.C0101/B1A0102
SD_DAT2
SD_DAT3
SD_CMD
SD_CLK
SD_DAT0
SD_DAT1
R333 51K
R294 51K
R323 51K
R312 51K
R305 51K
R309 51K
R335 NO-POP
R288 NO-POP
R329 NO-POP
8 SD0_DAT2
8 SD0_DAT3
8 SD0_CMD
8 SD0_CLK
8 SD0_DAT0
8 SD0_DAT1

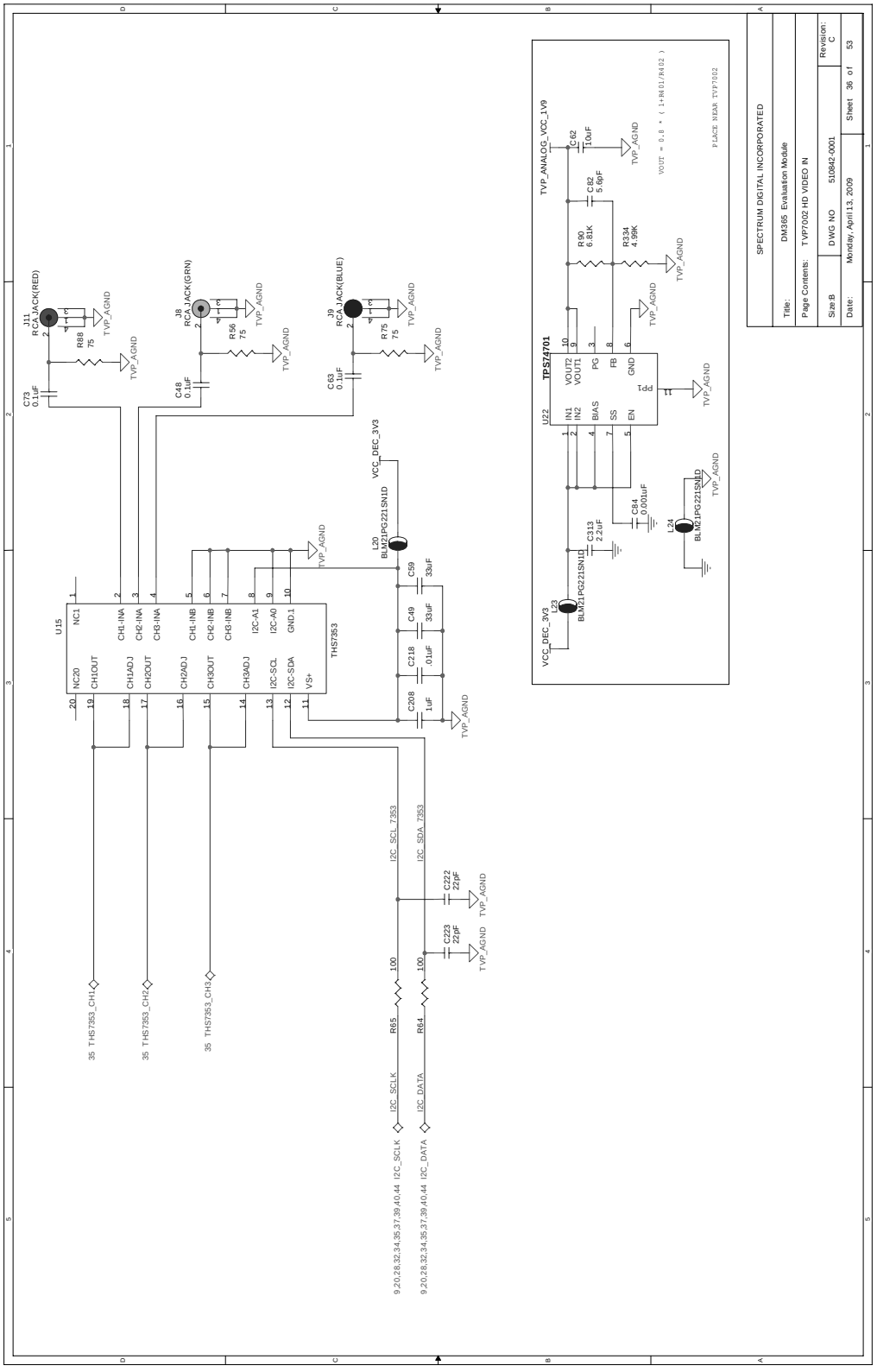

SPECTRUM DIGITAL INCORPORATED
Title: DM365 Evaluation Module
Page Contents: SD/MMC CARD INTERFACE
Size:B
DWG NO 506902-0001
Revision:
Date: Monday, April 13, 2009
Sheet 31 of 53
SD/MMC1.WP 23
SD/MMC1.INS 23
VCC_3V3
R325 51K
R336 51K
R331 0
WP
CD
CD
J25
CARD_DETECT
MMC/SD_CARD
DAT2
DAT3
CMD
VSS1
VDD
CLK
VSS2
DAT0
DAT1
C310 .1uF
C311 10uF
CONN_SD1_DAT2
CONN_SD1_DAT3
CONN_SD1_CMD
CONN_SD1_CLK
CONN_SD1_DAT0
CONN_SD1_DAT1
R307 51K
R289 51K
R281 51K
R67 51K
R319 51K
R313 51K
R310 NO-POP
R297 NO-POP
R285 NO-POP
8 CONN_SD1_DAT2
8 CONN_SD1_DAT3
8 CONN_SD1_CMD
8 CONN_SD1_CLK
8 CONN_SD1_DAT0
8 CONN_SD1_DAT1

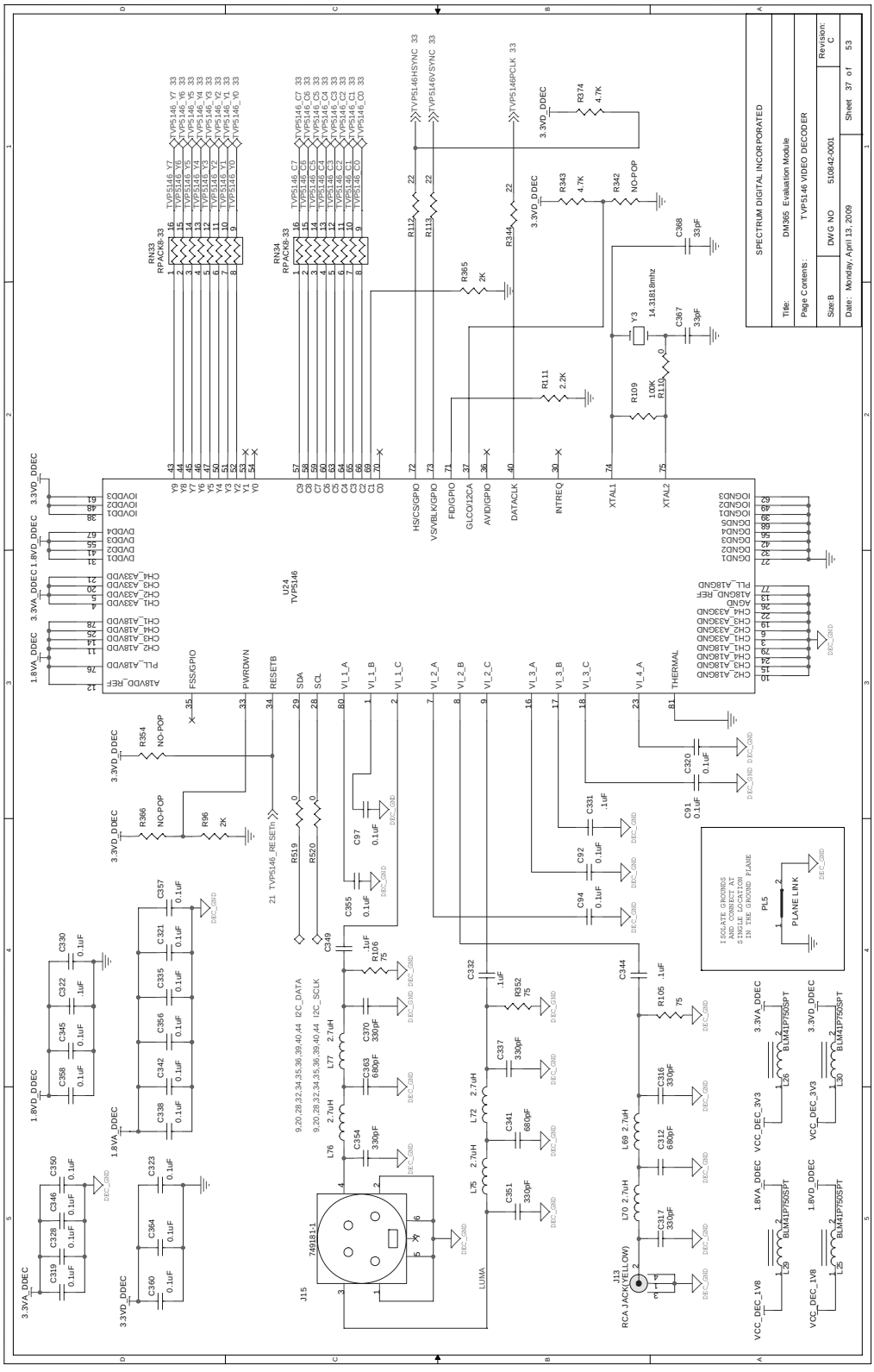

SPECTRUM DIGITAL INCORPORATED
Title: DM365 Evaluation Module
Page Contents: COMPONENT VIDEO OUTPUT
Size:B DWG NO 510842-0001 Revision: C
Date: Monday, April 13, 2009 Sheet 32 of 53
J21 RCA JACK(RED)
J17 RCA JACK(GRN)
J20 RCA JACK(BLUE)
U23 THS7303
VCC_3V3
VCC_DENC
I2C_SDA_7303
I2C_SCL_7303
I2C_DATA
I2C_SCLK
PLANE LINK
DENC_GND

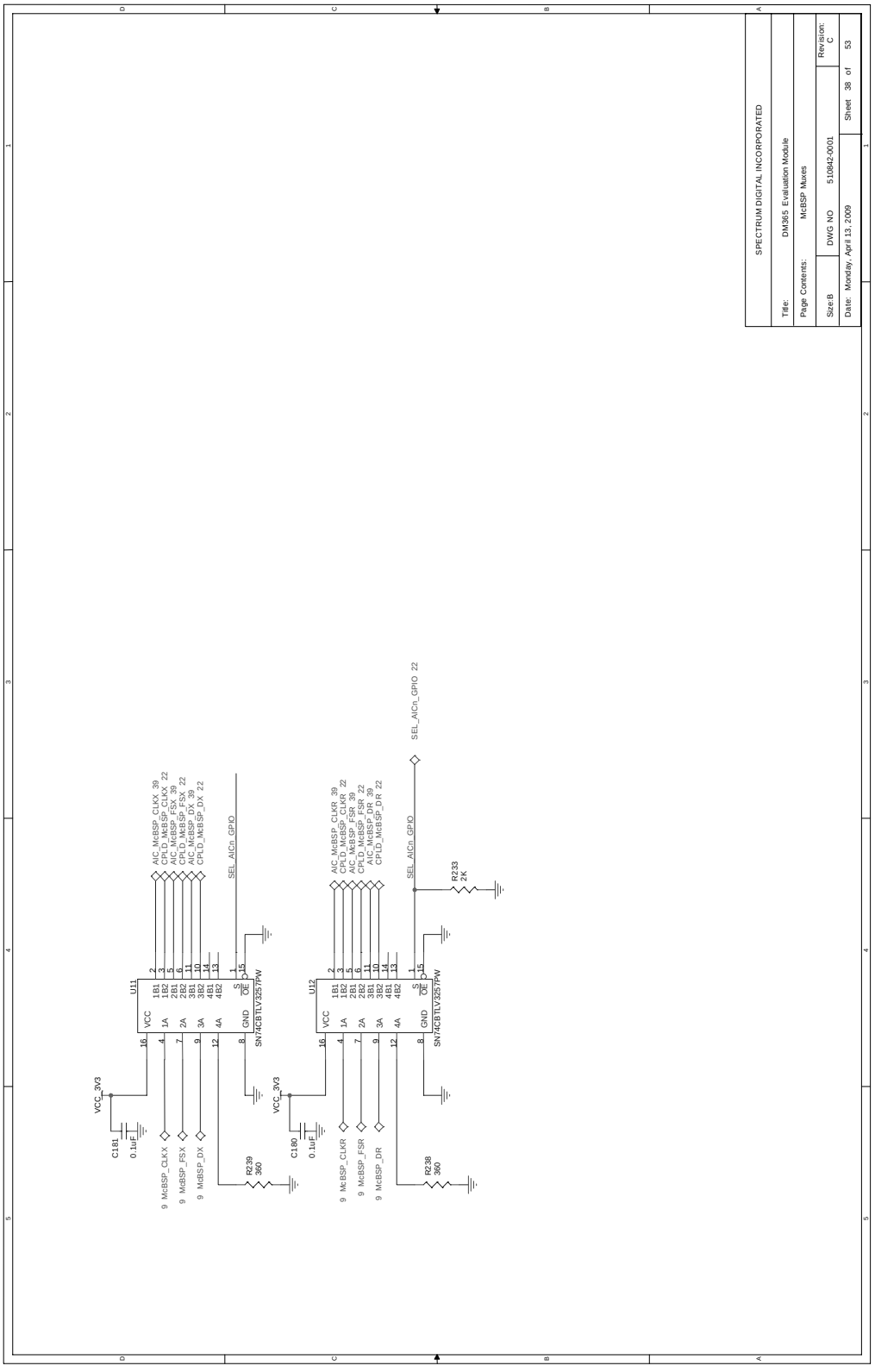

SPECTRUM DIGITAL INCORPORATED
Title: DM365 Evaluation Module
Page Contents: VIDEO INPUT MULTIPLEXER
Size:B DWG NO 510842-0001 Revision: C
Date: Monday, April 13, 2009 Sheet 33 of 53
VCC_5V
R63
15K
D6
LM4040DCIM3-4.1
VID_4V1
U17
U21
SN74CBT16214DGGR
DECODER_IMAGER_S0
DECODER_IMAGER_S1
DECODER_IMAGER_S2
R296
R298
R295
R301
R328
360
10K
C250
560pF
C251
0.1uF
C299
C300
RN26
RPACK4-33
HD_CLKIN
CCD_PCLK
CCD_HSYNC
CCD_VSYNC
TVP5146_Y7
TVP5146_Y6
TVP5146_Y5
TVP5146_Y4
TVP5146_Y3
TVP5146_Y2
TVP5146_Y1
TVP5146_Y0
TVP5146VSYNC
TVP5146HSYNC
TVP5146PCLK
VDIN_PCLK
VDIN_HD
VDIN_VD
CPLD_CCD_DATA03
CPLD_CCD_DATA02
CPLD_CCD_DATA01
CPLD_CCD_DATA00

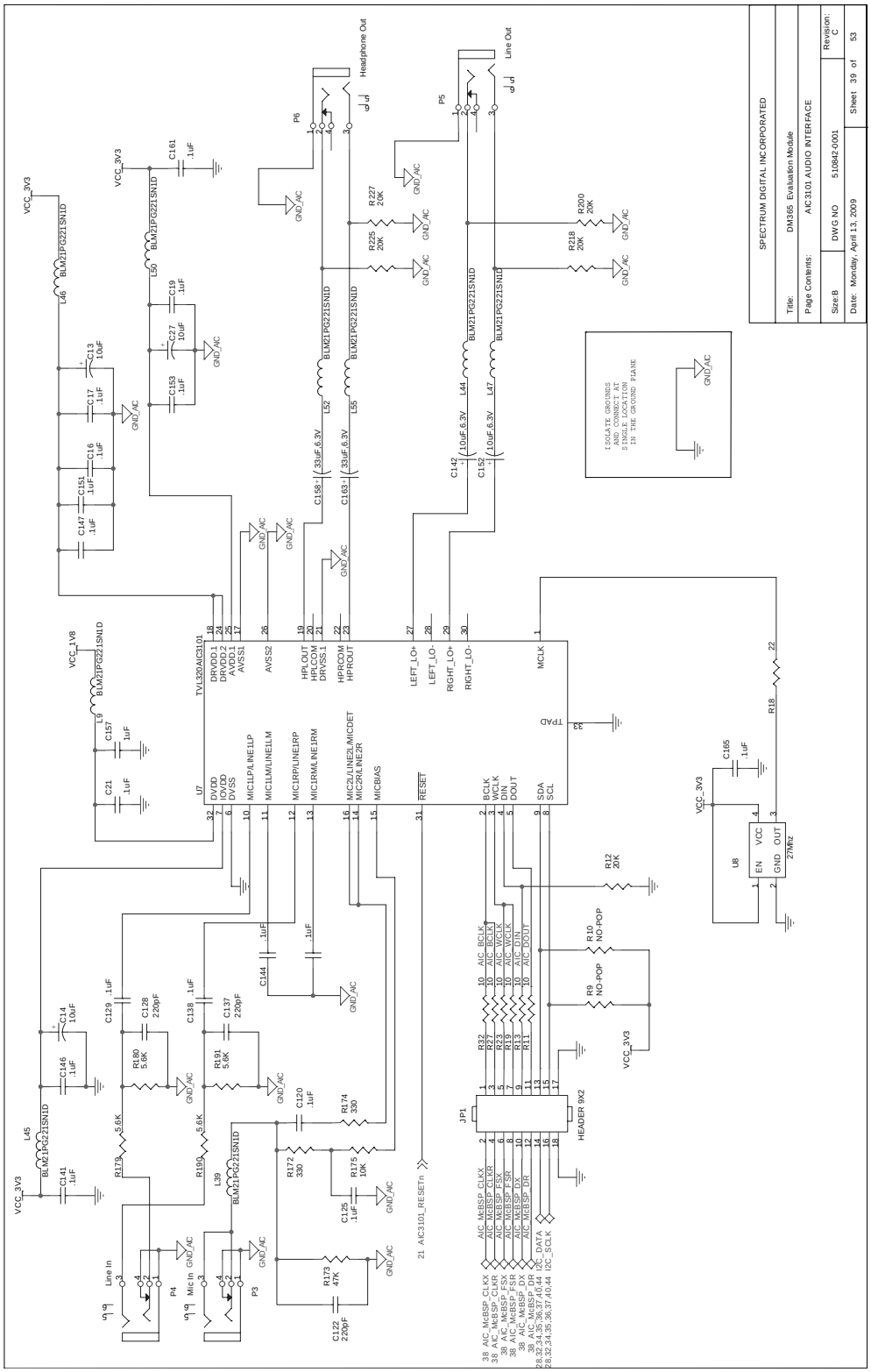

SPECTRUM DIGITAL INCORPORATED
Title: DM365 Evaluation Module
Page Contents: IMAGER INTERFACE
Size: B
DWG NO 510842-0001
Revision: C
Date: Monday, April 13, 2009
Sheet 34 of 53
J10A
J10B
J10C
PCN10-96P-2.54DSA,HIROSE CL583-0002-4
PCN10-96P-2.54DSA-HIROSE CL583-0002-4
5V_DC_J6
3V3_STB
3V3A_CCD
3V3_CCD
VCC_CCD15V
VCC_CCD_N7V5
VCC_5V
VCC_3V3
AFE_3V3
AGND_IMAGER
GND_STB
GND_MTR
MTR_3V3
CCD_PSMON
BLM41P750SPT
L48
L53
L68
L71
L74
L78
L81
C85 3.3uF
C90 3.3uF
C75 3.3uF
C329 0.01uF
C287 0.01uF
C306 0.01uF
C265 0.01uF
C271 0.01uF
C259 10uF
C278 10uF
R515 0
R516 0
I2C_DATA
I2C_SCLK

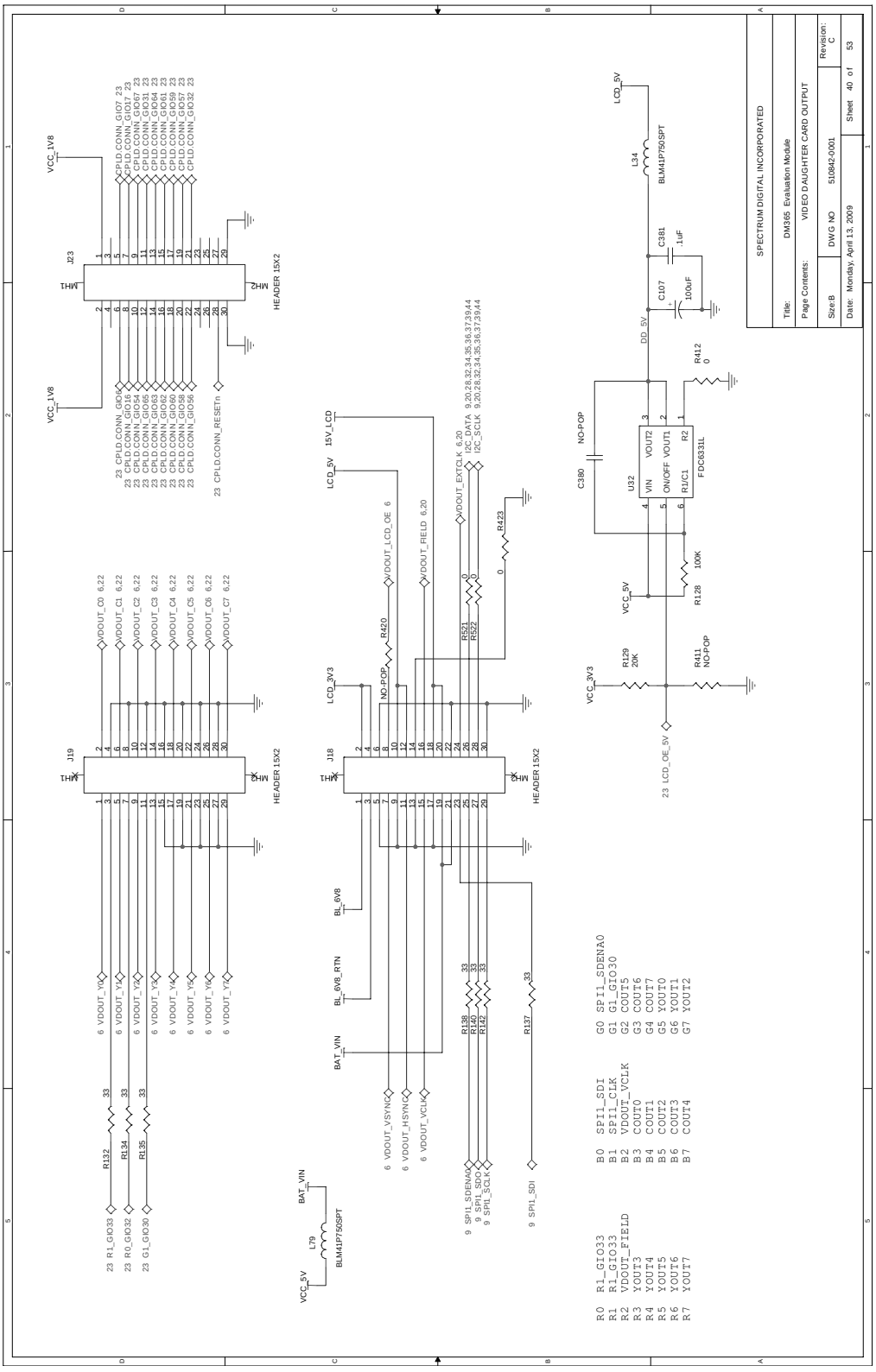

SPECTRUM DIGITAL INCORPORATED
Title: DM365 Evaluation Module
Page Contents: TVP7002 HD VIDEO IN
Size:B
DWG NO 510842-0001
Revision: C
Date: Monday, April 13, 2009
Sheet 35 of 53
U20
TVP7002
THS7353_CH1
THS7353_CH2
THS7353_CH3
TVP_AVCC_3V3
TVP_AVCC_1V8
TVP_VCC_PLL
TVP_AGND
VCC_3V3
VCC_1V8
VCC_DEC_3V3
TVP_ANALOG_VCC_1V9
L21
BLM21PG221SN1D
FIDOUT
VSOUT
HSOUT
SOGOUT
DATACLK
EXT_CLK
RESETB
SDA
SCL
I2CA
COAST
CLAMP
PWDN
TMS
HD_VSYNC
HD_HSYNC
HD_CLKIN
TVP_7002_RSTn
I2C_DATA
I2C_SCLK
NO-POP
1.5K 1%

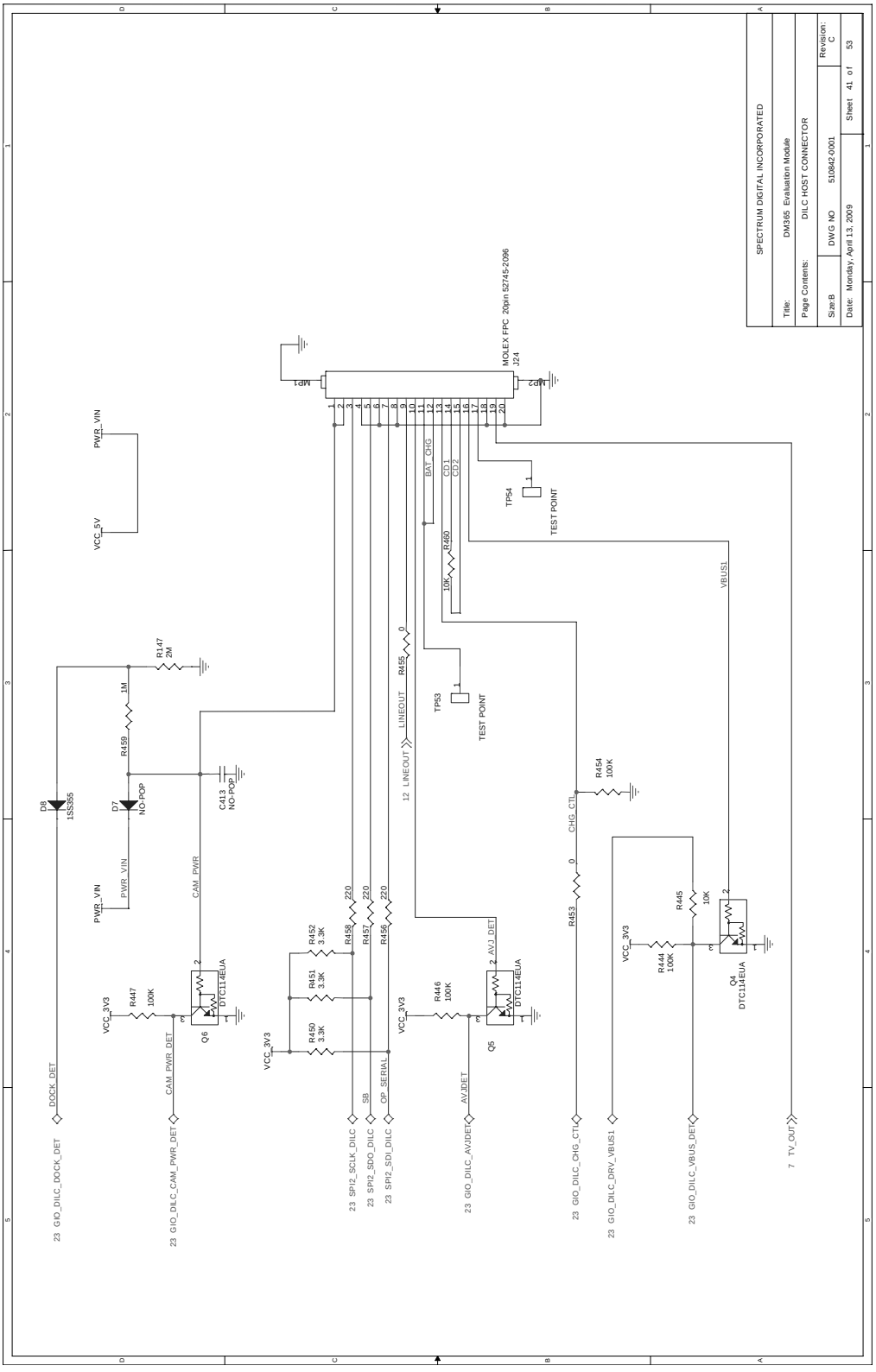

SPECTRUM DIGITAL INCORPORATED
Title: DM365 Evaluation Module
Page Contents: TVP7002 HD VIDEO IN
Size: B
DWG NO 510842-0001
Revision: C
Date: Monday, April 13, 2009
Sheet 36 of 53
TVP_ANALOG_VCC_1V9
TPS74701
U15
THS7353
VCC_DEC_3V3
TVP_AGND
I2C_SCL_7353
I2C_SDA_7353
I2C_SCLK
I2C_DATA

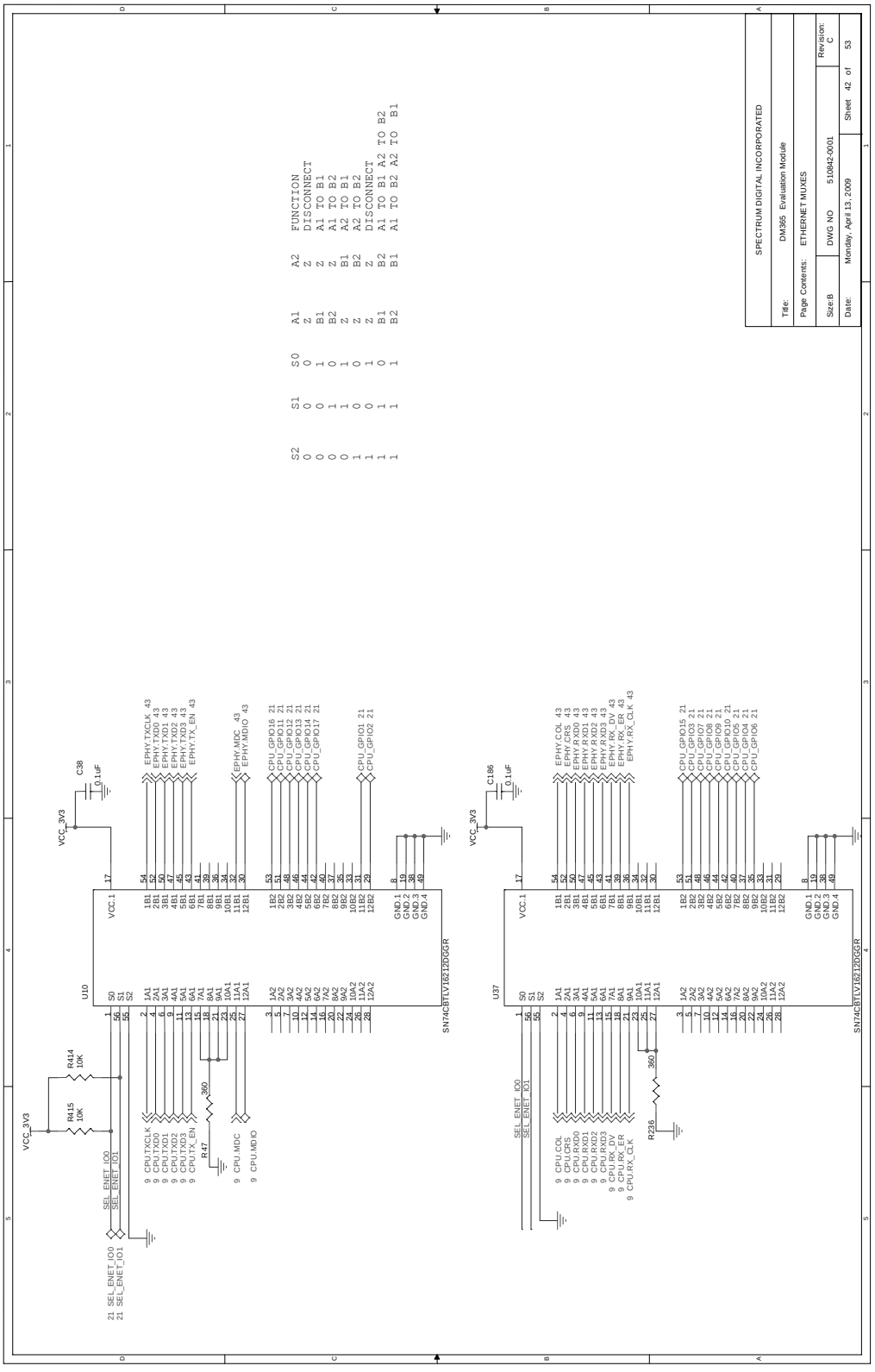

SPECTRUM DIGITAL INCORPORATED
Title: DM365 Evaluation Module
Page Contents: TVP5146 VIDEO DECODER
Size: B
DWG NO 510842-0001
Revision: C
Date: Monday, April 13, 2009
Sheet 37 of 53
U24 TVP5146
RN33 RPACK8-33
RN34 RPACK8-33
Y3 14.31818mhz
J15 74918-1-1
J13 RCA JACK(YELLOW)
PL5 PLANE LINK
ISOLATE GROUNDS AND CONNECT AT A SINGLE LOCATION IN THE GROUND PLANE

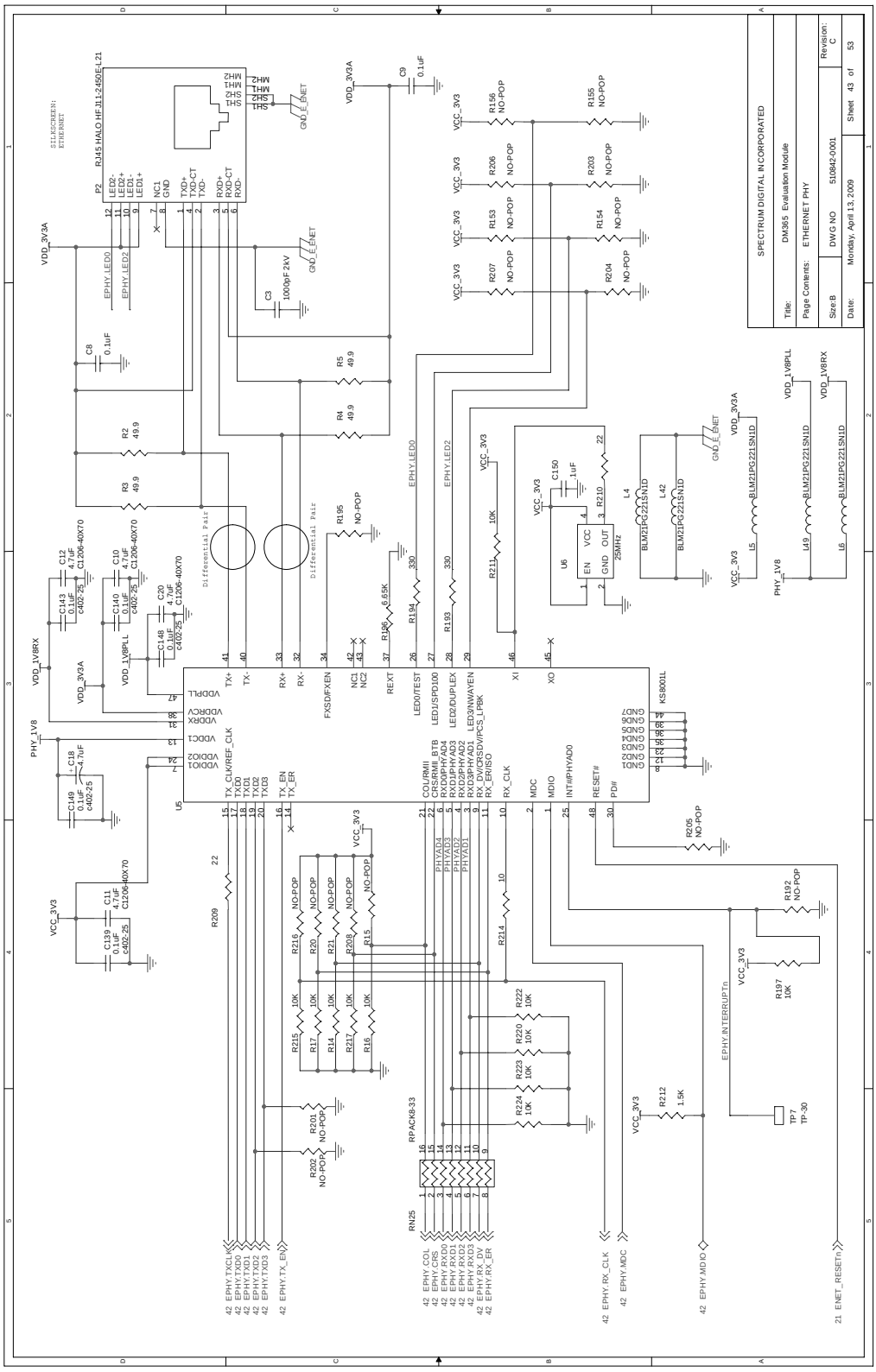

SPECTRUM DIGITAL INCORPORATED
Title: DM365 Evaluation Module
Page Contents: McBSP Muxes
Size: B
DWG NO 510842-0001
Revision: C
Date: Monday, April 13, 2009
Sheet 38 of 53
U11
U12
SN74CBTLV3257PW
VCC_3V3
C181
C180
0.1uF
R239
R238
360
R233
2K
SEL_AICn_GPIO
SEL_AICn_GPIO 22
AIC_McBSP_CLKX 39
CPLD_McBSP_CLKX 22
AIC_McBSP_FSX 39
CPLD_McBSP_FSX 22
AIC_McBSP_DX 39
CPLD_McBSP_DX 22
AIC_McBSP_CLKR 39
CPLD_McBSP_CLKR 22
AIC_McBSP_FSR 39
CPLD_McBSP_FSR 22
AIC_McBSP_DR 39
CPLD_McBSP_DR 22
9 McBSP_CLKX
9 McBSP_FSX
9 McBSP_DX
9 McBSP_CLKR
9 McBSP_FSR
9 McBSP_DR

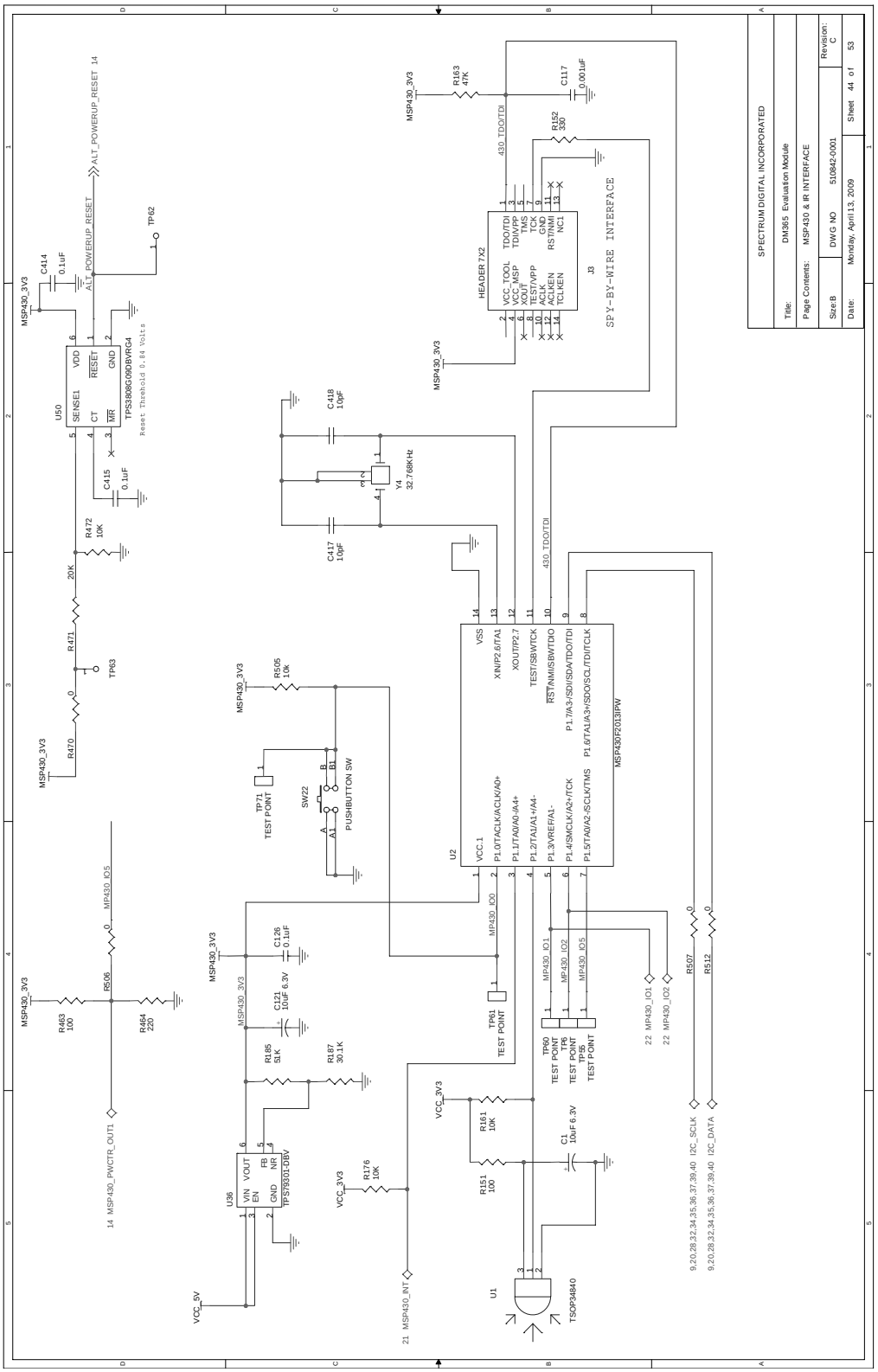

SPECTRUM DIGITAL INCORPORATED
Title: DM365 Evaluation Module
Page Contents: AIC3101 AUDIO INTERFACE
Size:B
DWG NO 510842-0001
Revision: C
Date: Monday, April 13, 2009
Sheet 39 of 53
TVL320AIC3101
U7
HEADER 9X2
JP1
Headphone Out
Line Out
Line In
Mic In
ISOLATE GROUNDS AND CONNECT AT SINGLE LOCATION TO THE GROUND PLANE

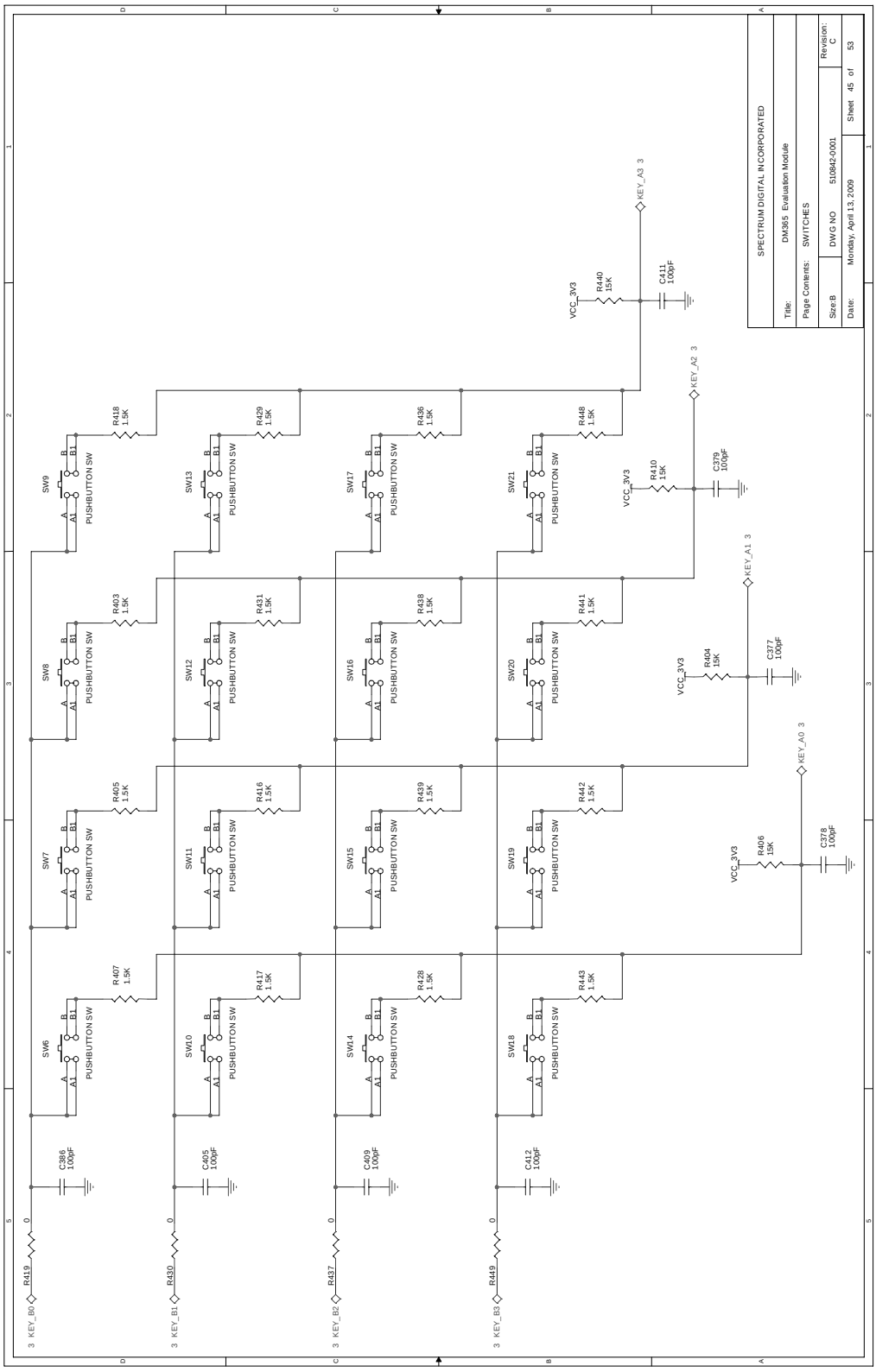

SPECTRUM DIGITAL INCORPORATED
Title: DM365 Evaluation Module
Page Contents: VIDEO DAUGHTER CARD OUTPUT
Size: B
DWG NO 510942-0001
Revision: C
Date: Monday, April 13, 2009
Sheet 40 of 53
J23
HEADER 15X2
J19
HEADER 15X2
J18
HEADER 15X2
VCC_1V8
LCD_5V
15V_LCD
LCD_3V3
VCC_5V
BAT_VIN
BL_6V8
BL_6V8_RTN
U32
FDC6331L
L34
BLM41P750SPT
L79
BLM41P750SPT
C380
NO-POP
C381
.1uF
C107
100uF
R412
0
R411
NO-POP
R129
20K
R128
100K
R420
NO-POP
R423
R521
R522
R132
R134
R135
R137
R138
R140
R142
VDOUT_EXTCLK 6,20
I2C_DATA 9,20,28,32,34,35,36,37,39,44
I2C_SCLK 9,20,28,32,34,35,36,37,39,44
VDOUT_LCD_OE 6
VDOUT_RELD 6,20
23 LCD_OE_5V
6 VDOUT_VSYNC
6 VDOUT_HSYNC
6 VDOUT_VCLK
9 SPI1_SDENA0
9 SPI1_SDO
9 SPI1_SCLK
9 SPI1_SDI
23 R1_GIO33
23 R0_GIO32
23 G1_GIO30
23 CPLD.CONN_RESETn
R0 R1_GIO33
R1 R1_GIO33
R2 VDOUT_FIELD
R3 YOUT3
R4 YOUT4
R5 YOUT5
R6 YOUT6
R7 YOUT7
B0 SPI1_SDI
B1 SPI1_CLK
B2 VDOUT_VCLK
B3 COUT0
B4 COUT1
B5 COUT2
B6 COUT3
B7 COUT4
G0 SPI1_SDENA0
G1 G1_GIO30
G2 COUT5
G3 COUT6
G4 COUT7
G5 YOUT0
G6 YOUT1
G7 YOUT2

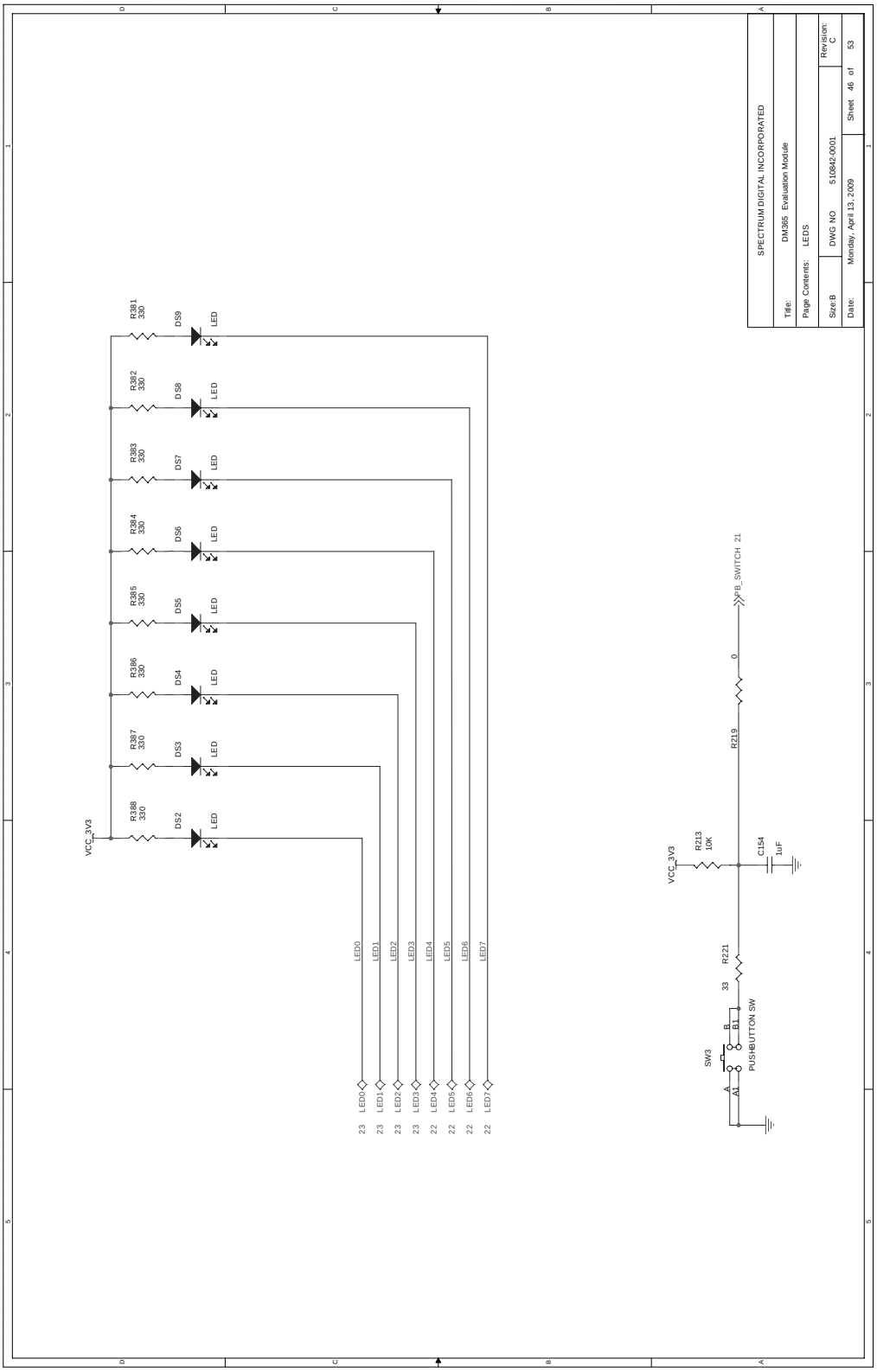

SPECTRUM DIGITAL INCORPORATED
Title: DM365 Evaluation Module
Page Contents: DILC HOST CONNECTOR
Size: B
DWG NO 510842-0001
Revision: C
Date: Monday, April 13, 2009
Sheet 41 of 53
MOLEX FPC 20pin 52745-2096
J24
TEST POINT
TP54
TP53
R460
10K
R455
0
R459
1M
R147
2M
R447
100K
R446
100K
R444
100K
R445
10K
R454
100K
R453
0
R452
3.3K
R451
3.3K
R450
3.3K
R458
220
R457
220
R456
220
D8
1SS355
D7
NO-POP
C413
NO-POP
Q6
Q5
Q4
DTC114EUA
PWR_VIN
VCC_5V
VCC_3V3
CAM_PWR
CAM_PWR_DET
DOCK_DET
CHG_CTL
VBUS1
BAT_CHG
CD1
CD2
LINEOUT
AVJ_DET
SB
OP_SERIAL
TV_OUT
23 GIO_DILC_DOCK_DET
23 GIO_DILC_CAM_PWR_DET
23 SPI2_SCLK_DILC
23 SPI2_SDO_DILC
23 SPI2_SDI_DILC
23 GIO_DILC_AVJDET
23 GIO_DILC_CHG_CTL
23 GIO_DILC_DRV_VBUS1
23 GIO_DILC_VBUS_DET
12 LINEOUT
7 TV_OUT

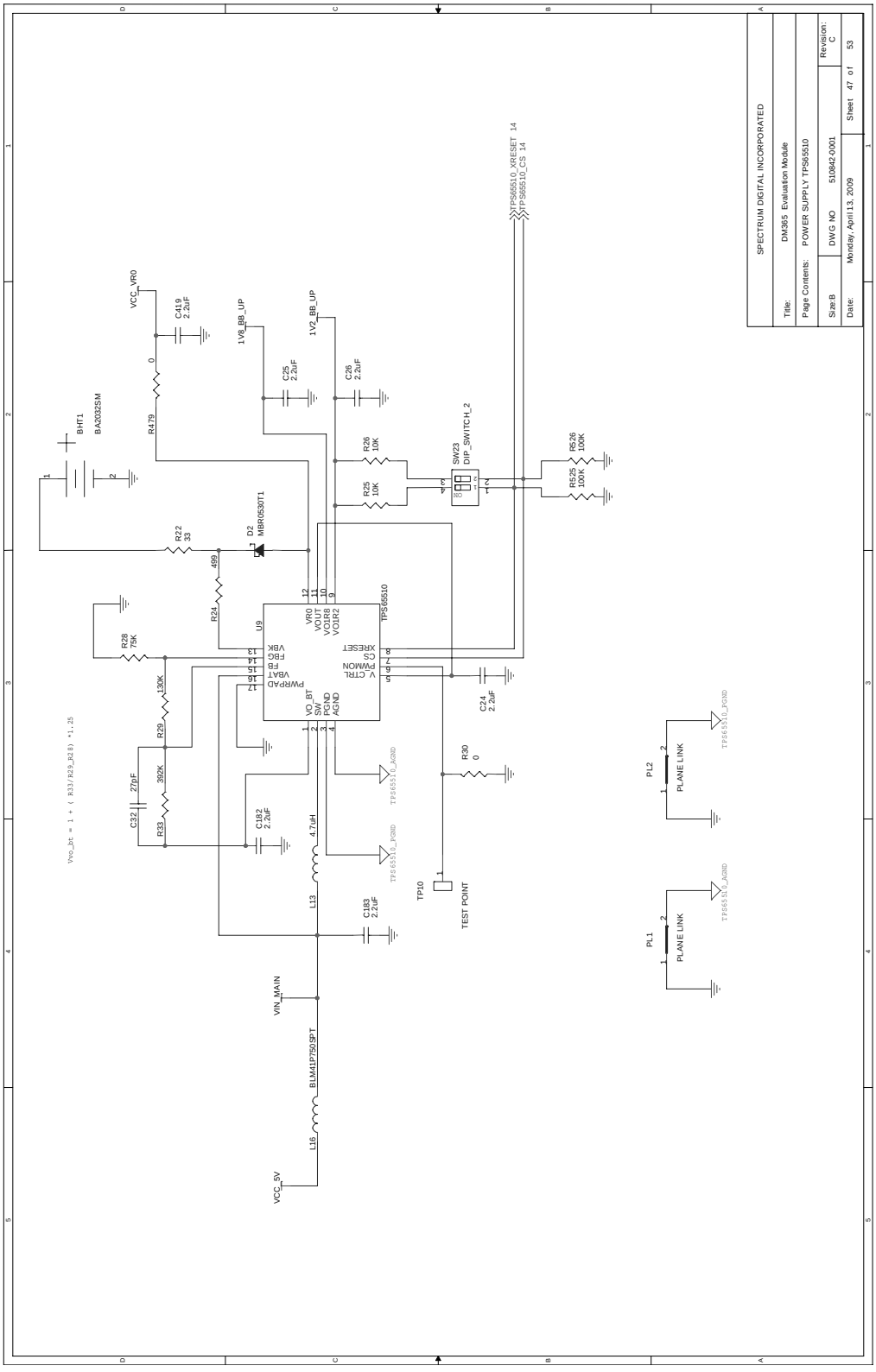

SPECTRUM DIGITAL INCORPORATED
Title: DM365 Evaluation Module
Page Contents: ETHERNET MUXES
Size:B DWG NO 510842-0001 Revision: C
Date: Monday, April 13, 2009 Sheet 42 of 53
S2 S1 S0 A1 A2 FUNCTION
0 0 0 Z Z DISCONNECT
0 0 1 B1 Z A1 TO B1
0 1 0 B2 Z A1 TO B2
0 1 1 Z B1 A2 TO B1
1 0 0 Z B2 A2 TO B2
1 0 1 Z Z DISCONNECT
1 1 0 B1 B2 A1 TO B2 A2 TO B1
1 1 1 B2 B1 A1 TO B2 A2 TO B1
U10
U37
SN74CBTLV16212DGGR
VCC_3V3
C38
C186
0.1uF
R414 10K
R415 10K
R47 360
R236 360
SEL_ENET_IO0
SEL_ENET_IO1
EPHY.TXCLK 43
EPHY.TXD0 43
EPHY.TXD1 43
EPHY.TXD2 43
EPHY.TXD3 43
EPHY.TX_EN 43
EPHY.MDC 43
EPHY.MDIO 43
EPHY.COL 43
EPHY.CRS 43
EPHY.RXD0 43
EPHY.RXD1 43
EPHY.RXD2 43
EPHY.RXD3 43
EPHY.RX_DV 43
EPHY.RX_ER 43
EPHY.RX_CLK 43
CPU_GPIO16 21
CPU_GPIO11 21
CPU_GPIO12 21
CPU_GPIO13 21
CPU_GPIO14 21
CPU_GPIO17 21
CPU_GPIO1 21
CPU_GPIO2 21
CPU_GPIO15 21
CPU_GPIO3 21
CPU_GPIO7 21
CPU_GPIO8 21
CPU_GPIO9 21
CPU_GPIO10 21
CPU_GPIO5 21
CPU_GPIO4 21
CPU_GPIO6 21
CPU.TXCLK
CPU.TXD0
CPU.TXD1
CPU.TXD2
CPU.TXD3
CPU.TX_EN
CPU.MDC
CPU.MDIO
CPU.COL
CPU.CRS
CPU.RXD0
CPU.RXD1
CPU.RXD2
CPU.RXD3
CPU.RX_DV
CPU.RX_ER
CPU.RX_CLK

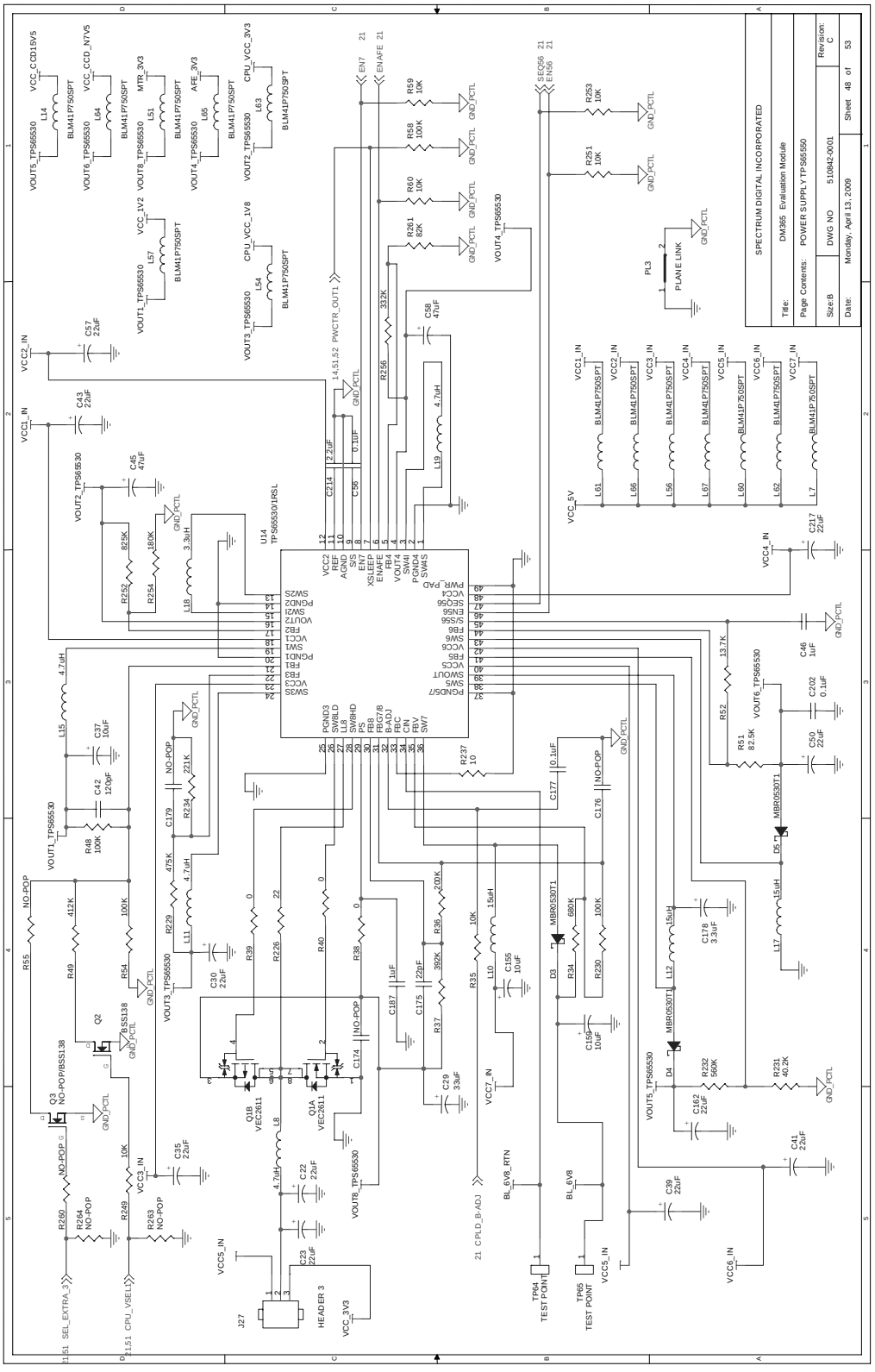

SPECTRUM DIGITAL INCORPORATED
Title: DM365 Evaluation Module
Page Contents: ETHERNET PHY
Size:B
DWG NO 510842-0001
Revision: C
Date: Monday, April 13, 2009
Sheet 43 of 53
P2 RJ45 HALO HFJ11-2450E-L21
U5
U6
RN25
RPACK8-33
SILKSCREEN: ETHERNET
Differential Pair
EPHY.LED0
EPHY.LED2
EPHY.INTERRUPTn
EPHY.TXCLK
EPHY.TXD0
EPHY.TXD1
EPHY.TXD2
EPHY.TXD3
EPHY.TX_EN
EPHY.COL
EPHY.CRS
EPHY.RXD0
EPHY.RXD1
EPHY.RXD2
EPHY.RXD3
EPHY.RX_DV
EPHY.RX_ER
EPHY.RX_CLK
EPHY.MDC
EPHY.MDIO
ENET_RESETn
GND_E_NET
VDD_3V3A
VCC_3V3
PHY_1V8
VDD_1V8PLL
VDD_1V8RX
VDD_1V8RX
VDD_3V3A
PHY_1V8
VDD_1V8PLL
VDD_1V8RX

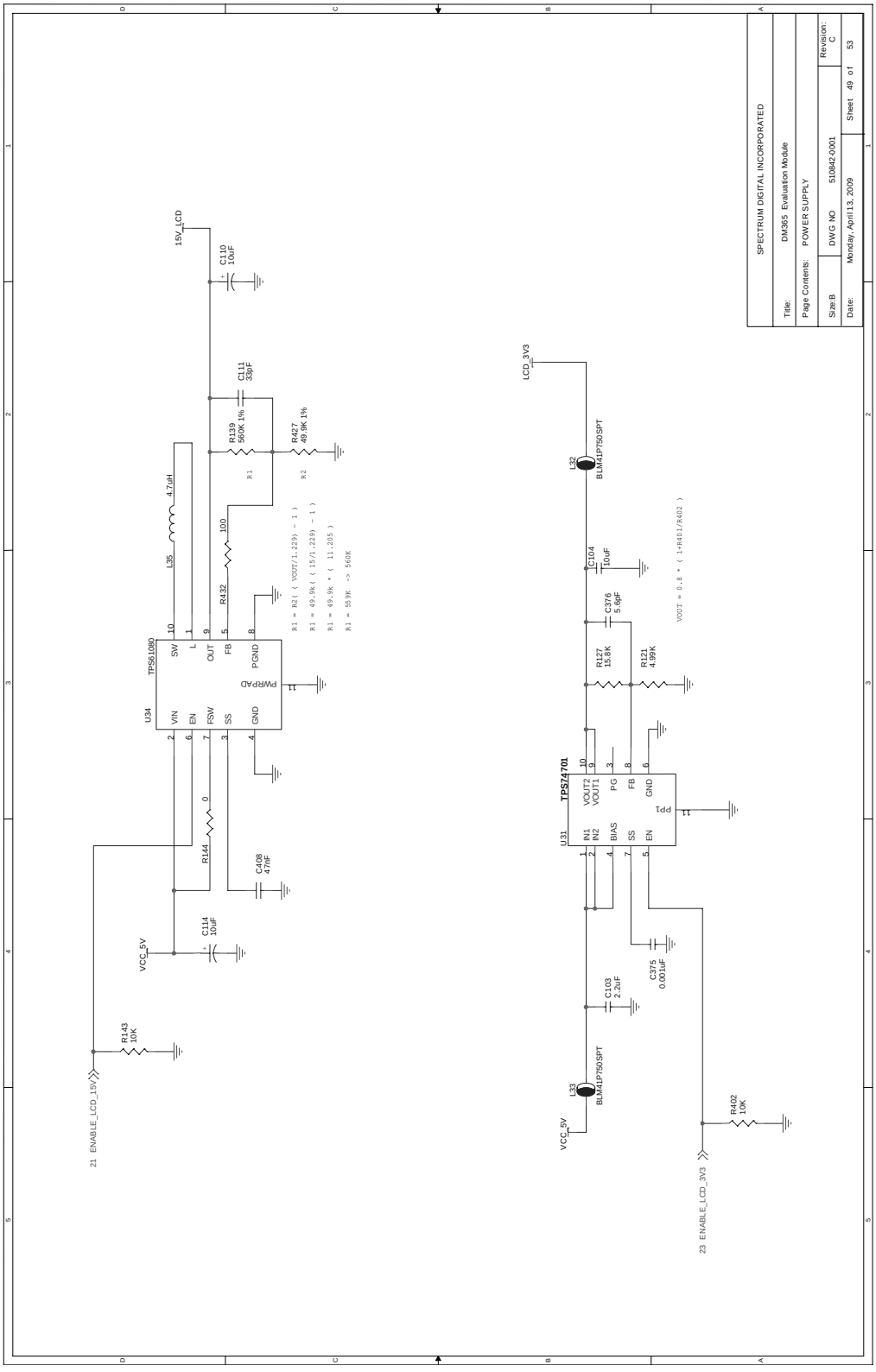

SPECTRUM DIGITAL INCORPORATED
Title: DM365 Evaluation Module
Page Contents: MSP430 & IR INTERFACE
Size:B
DWG NO 510842-0001
Revision: C
Date: Monday, April 13, 2009
Sheet 44 of 53
SPY-BY-WIRE INTERFACE
HEADER 7X2
MSP430F2013IPW
TSOP34840
TPS7830I-DBV
TPS3808G09DBVRG4
Reset Threshold 0.84 Volts

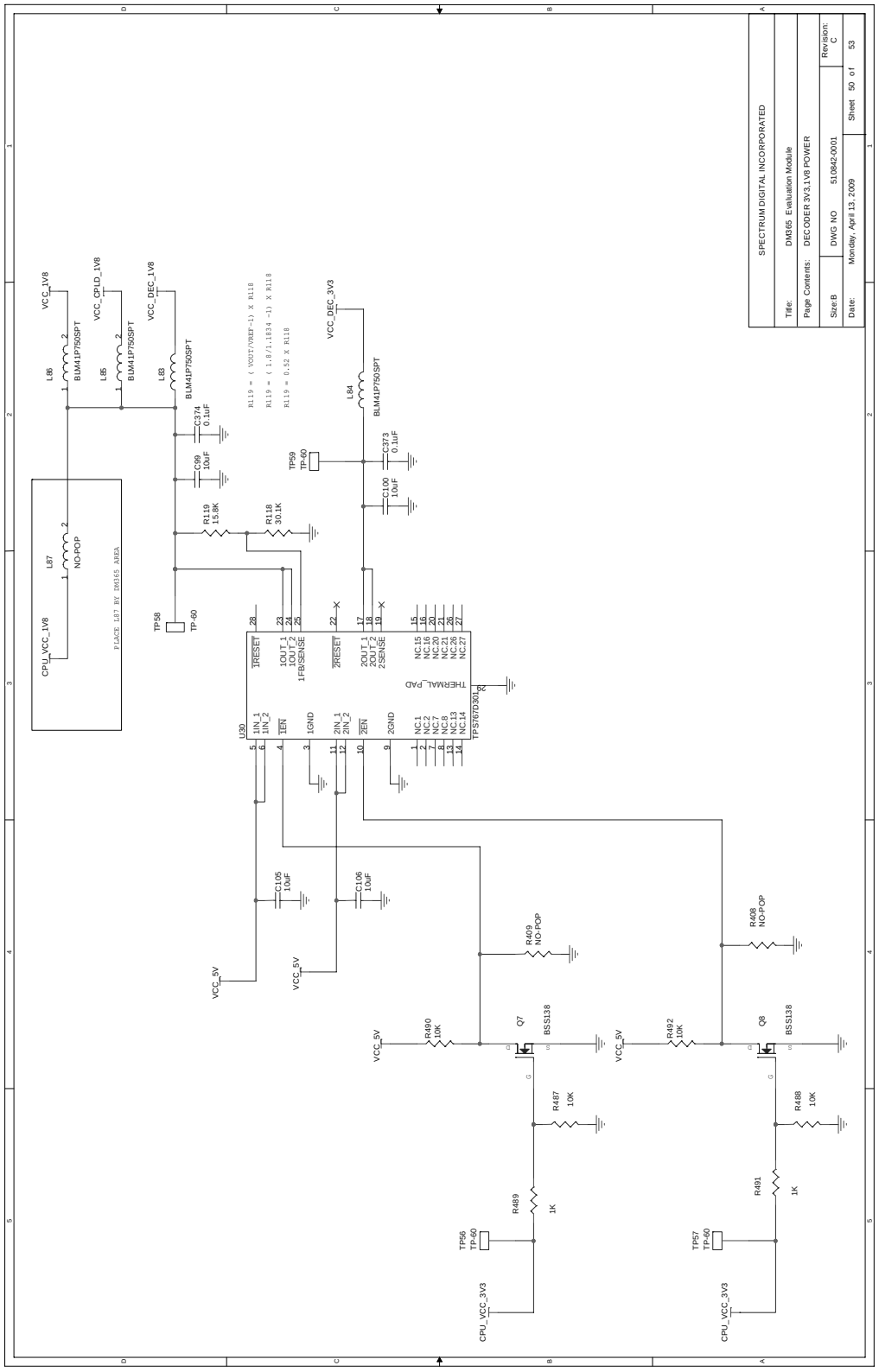

SPECTRUM DIGITAL INCORPORATED
Title: DM365 Evaluation Module
Page Contents: SWITCHES
Size:B
DWG NO 510842-0001
Revision: C
Date: Monday, April 13, 2009
Sheet 45 of 53
KEY_A3
KEY_A2
KEY_A1
KEY_A0
KEY_B0
KEY_B1
KEY_B2
KEY_B3
VCC_3V3
R440 15K
R410 15K
R404 15K
R406 15K
C411 100pF
C379 100pF
C377 100pF
C378 100pF
SW9
SW13
SW17
SW21
SW8
SW12
SW16
SW20
SW7
SW11
SW15
SW19
SW6
SW10
SW14
SW18
PUSHBUTTON SW
R418 1.5K
R429 1.5K
R436 1.5K
R448 1.5K
R403 1.5K
R431 1.5K
R438 1.5K
R441 1.5K
R405 1.5K
R416 1.5K
R439 1.5K
R442 1.5K
R407 1.5K
R417 1.5K
R428 1.5K
R443 1.5K
R419 0
R430 0
R437 0
R449 0
C386 100pF
C405 100pF
C409 100pF
C412 100pF

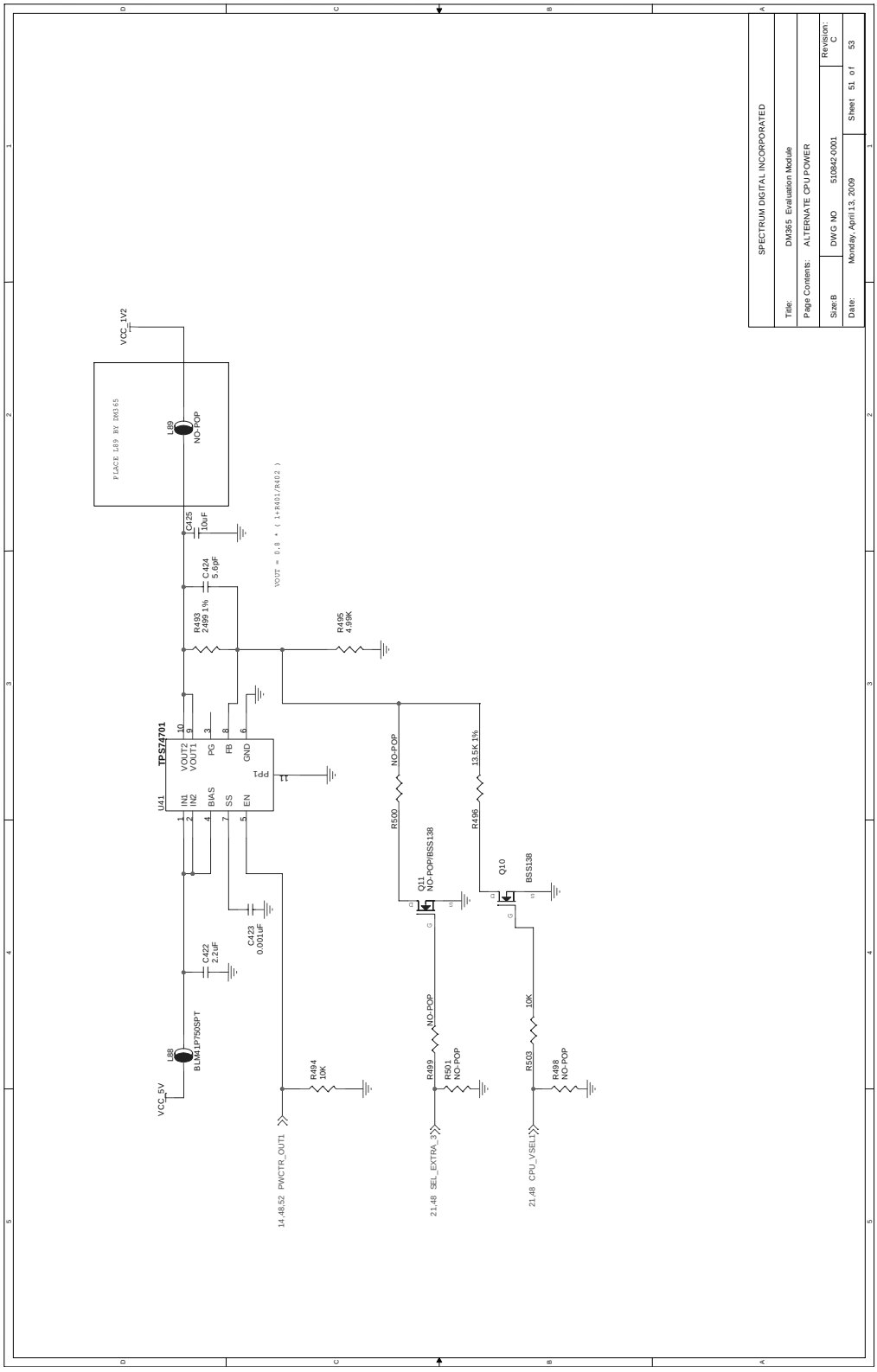

SPECTRUM DIGITAL INCORPORATED
Title: DM365 Evaluation Module
Page Contents: LEDS
Size:B
DWG NO 510842-0001
Revision: C
Date: Monday, April 13, 2009
Sheet 46 of 53
R381 330
DS9 LED
R382 330
DS8 LED
R383 330
DS7 LED
R384 330
DS6 LED
R385 330
DS5 LED
R386 330
DS4 LED
R387 330
DS3 LED
R388 330
DS2 LED
VCC_3V3
LED0
LED1
LED2
LED3
LED4
LED5
LED6
LED7
23 LED0
23 LED1
23 LED2
23 LED3
22 LED4
22 LED5
22 LED6
22 LED7
PB_SWITCH 21
R219 0
R213 10K
C154 1uF
VCC_3V3
R221 33
SW3
PUSHBUTTON SW

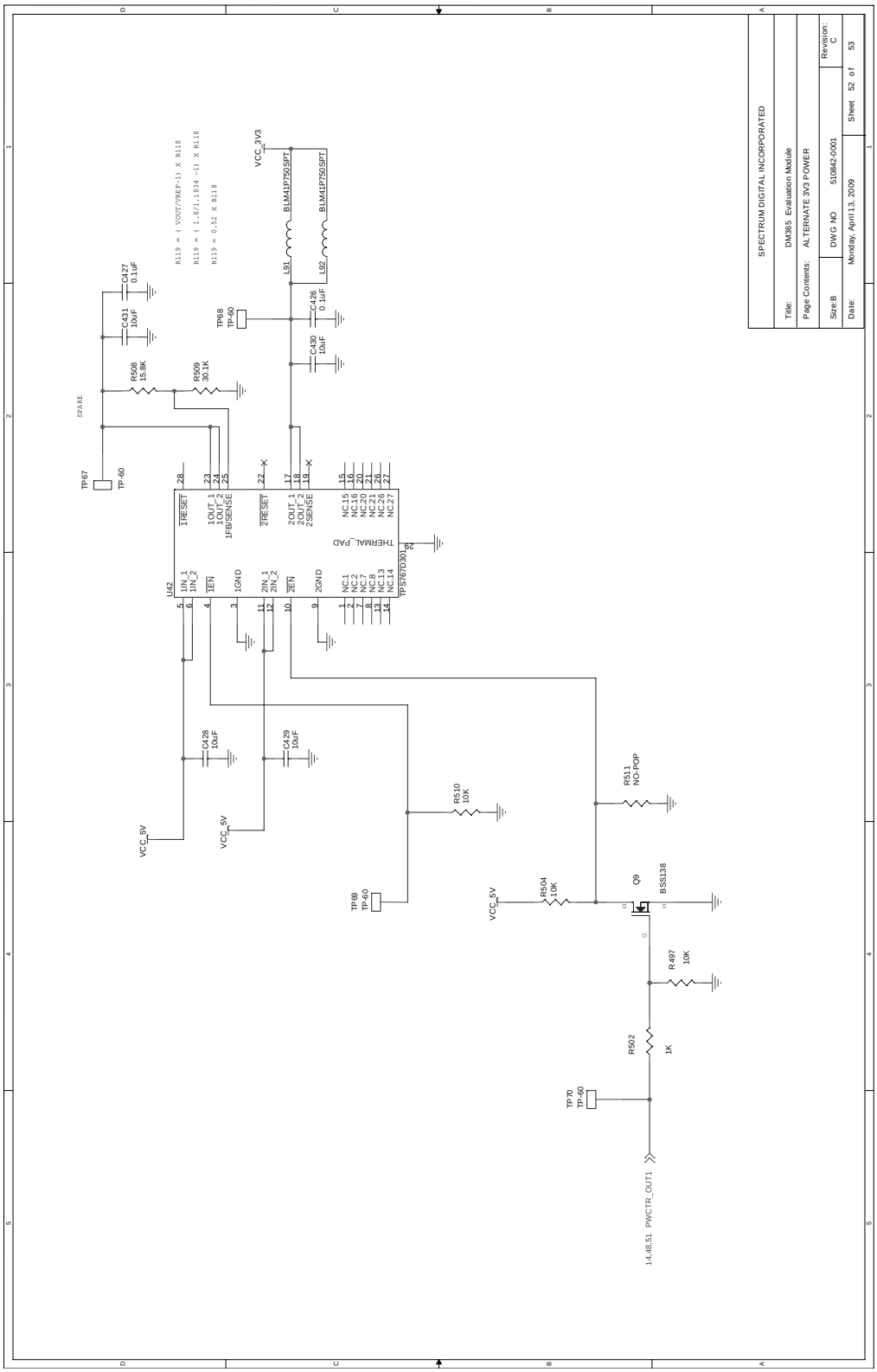

SPECTRUM DIGITAL INCORPORATED
Title: DM365 Evaluation Module
Page Contents: POWER SUPPLY TPS65510
Size: B
DWG NO 510842-0001
Revision: C
Date: Monday, April 13, 2009
Sheet 47 of 53
TPS65510_XRESET 14
TPS65510_CS 14
VCC_VR0
C419 2.2uF
1V8_BB_UP
1V2_BB_UP
C25 2.2uF
C26 2.2uF
BHT1
BA2032SM
R479
R26 10K
R25 10K
SW23
DIP_SWITCH_2
R526 100K
R525 100K
R22 33
D2
MBR0530T1
499
R24
U9
TPS65510
VR0
VOUT
VOUR8
VOUR2
R28 75K
130K
R29
27pF
392K
C32
R33
C182 2.2uF
4.7uH
L13
C183 2.2uF
C24 2.2uF
R30 0
TP10
TEST POINT
PL2
PLANE LINK
PL1
PLANE LINK
VIN_MAIN
BLM41P750SPT
L16
VCC_5V

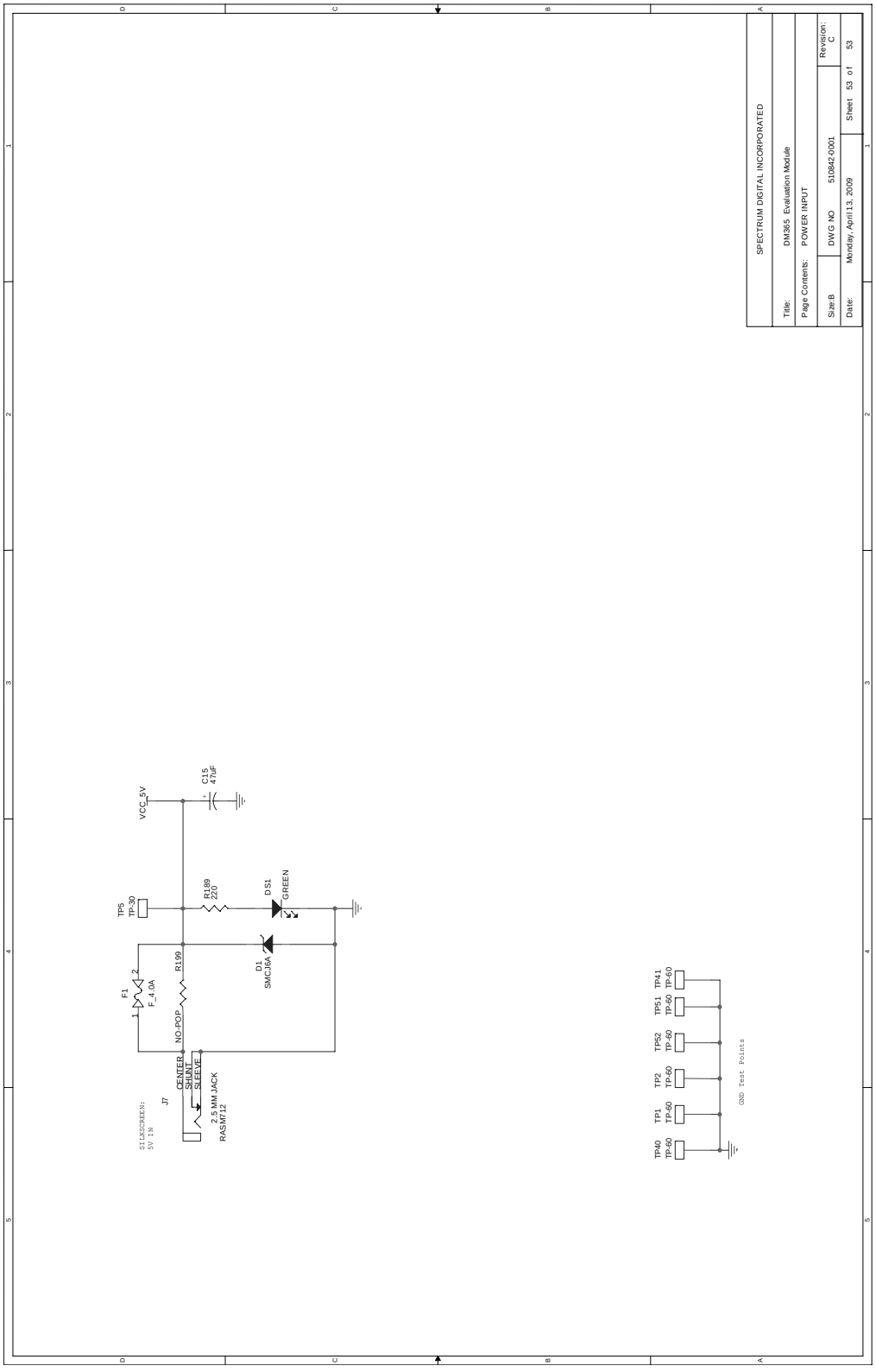

SPECTRUM DIGITAL INCORPORATED
Title: DM365 Evaluation Module
Page Contents: POWER SUPPLY TPS65550
Size: B
DWG NO 510842-0001
Revision: C
Date: Monday, April 13, 2009
Sheet 48 of 53
U14 TPS65530/1RSL
VCC2_IN
VCC1_IN
VCC_3V3
VCC5_IN
VCC6_IN
VCC7_IN
VCC4_IN
VCC_5V
VOUT1_TPS65530
VOUT2_TPS65530
VOUT3_TPS65530
VOUT4_TPS65530
VOUT5_TPS65530
VOUT6_TPS65530
VOUT8_TPS65530
BL_6V8
BL_6V8_RTN
CPLD_B-ADJ
PWCTR_OUT1
SEQ[5:0]
EN[6:0]
J27
HEADER 3
TP64 TEST POINT
TP65 TEST POINT
PL3
PLANE LINK
Q1A VEC2611
Q1B VEC2611
Q2 BSS138
Q3 NO-POP/BSS138
D3 MBR0530T1
D4 MBR0530T1
D5 MBR0530T1


SPECTRUM DIGITAL INCORPORATED
Title: DM365 Evaluation Module
Page Contents: POWER SUPPLY
Size: B
DWG NO 510842-0001
Revision: C
Date: Monday, April 13, 2009
Sheet 49 of 53
15V_LCD
C110 10uF
C111 33pF
R139 560K 1%
R427 49.9K 1%
L35 4.7uH
R432 100
U34 TPS61080
VIN
EN
FSW
SS
GND
SW
L
OUT
FB
P-GND
PWRPAD
R144 0
C408 47nF
C114 10uF
VCC_5V
R143 10K
21 ENABLE_LCD_15V
LCD_3V3
L32 BLM41P750SPT
C104 10uF
C376 5.6pF
R127 15.8K
R121 4.99K
U31 TPS74701
IN1
IN2
BIAS
SS
EN
VOUT2
VOUT1
PG
FB
GND
PPL
C103 2.2uF
C375 0.001uF
L33 BLM41P750SPT
R402 10K
23 ENABLE_LCD_3V3


SPECTRUM DIGITAL INCORPORATED
Title: DM365 Evaluation Module
Page Contents: DECODER 3V3,1V8 POWER
Size:B DWG NO 510842-0001 Revision: C
Date: Monday, April 13, 2009 Sheet 50 of 53
VCC_1V8
VCC_CPLD_1V8
VCC_DEC_1V8
VCC_DEC_3V3
L86 BLM41P750SPT
L85 BLM41P750SPT
L83 BLM41P750SPT
L84 BLM41P750SPT
L87 NO-POP
PLACE L87 BY DM365 AREA
CPU_VCC_1V8
C374 0.1uF
C99 10uF
C373 0.1uF
C100 10uF
R119 15.8K
R118 30.1K
TP58 TP-60
TP59 TP-60
U30 TPS767D301
C105 10uF
C106 10uF
VCC_5V
R409 NO-POP
R408 NO-POP
R490 10K
R492 10K
Q7 BSS138
Q8 BSS138
R487 10K
R488 10K
R489 1K
R491 1K
TP56 TP-60
TP57 TP-60
CPU_VCC_3V3


SPECTRUM DIGITAL INCORPORATED
Title: DM365 Evaluation Module
Page Contents: ALTERNATE CPU POWER
Size:B
DWG NO 510842-0001
Revision: C
Date: Monday, April 13, 2009
Sheet 51 of 53
VCC_1V2
PLACE L89 BY DM365
L89
NO-POP
C425
10uF
C424
5.6pF
R493
2.49K 1%
R495
4.99K
VOUT = 0.8 * (1+R401/R402)
U41
TPS74701
VOUT2
VOUT1
PG
PB
GND
IN1
IN2
BIAS
SS
EN
PPL
R500
NO-POP
R496
13.5K 1%
Q11
NO-POP/BSS138
Q10
BSS138
C422
2.2uF
C423
0.001uF
L88
BLM41P750SPT
VCC_5V
R494
10K
R499
NO-POP
R501
NO-POP
R503
10K
R498
NO-POP
14,48,52 PWCTR_OUT1
21,48 SEL_EXTRA_3V
21,48 CPU_VSEL1

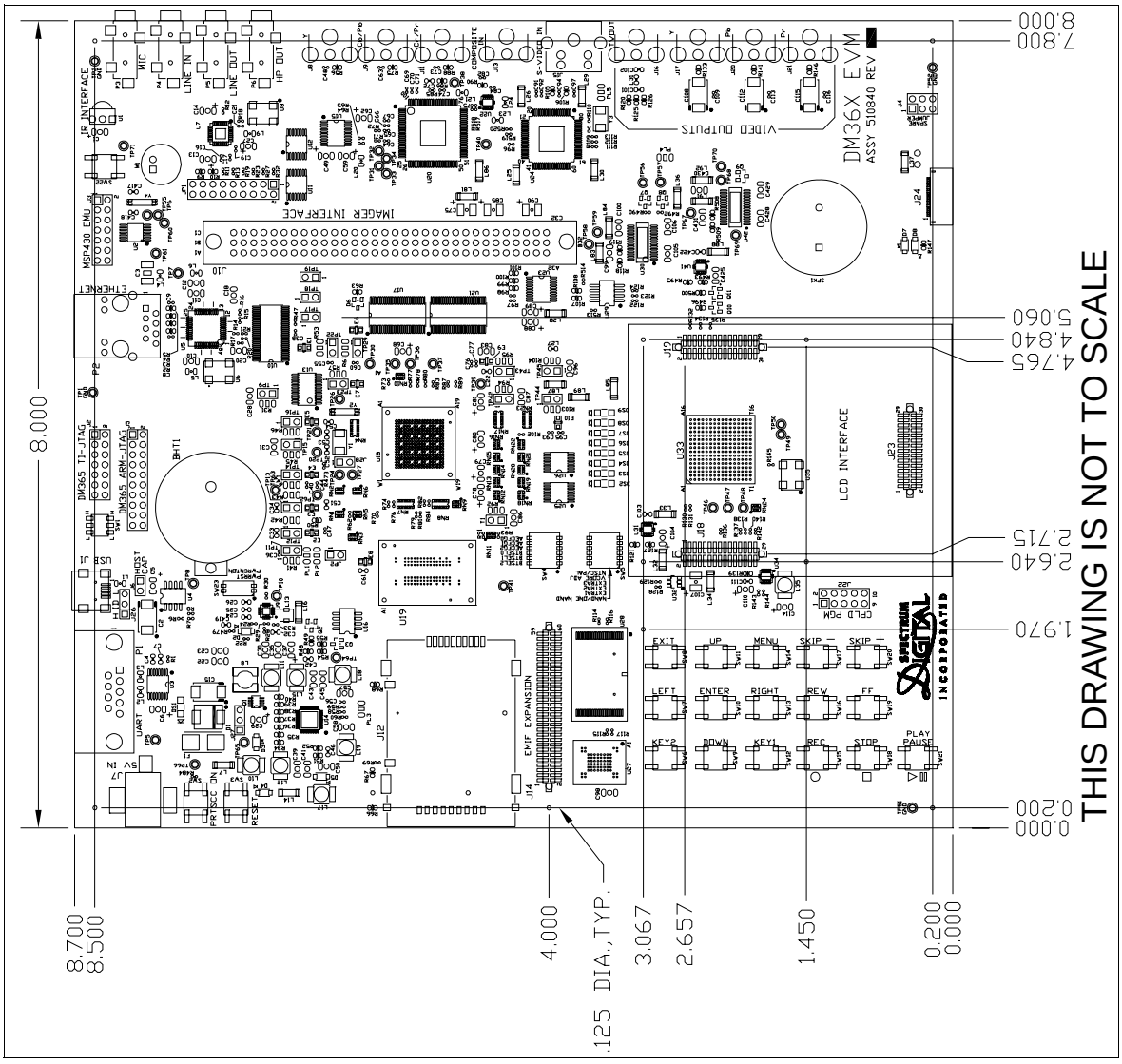

SPECTRUM DIGITAL INCORPORATED
Title: DM365 Evaluation Module
Page Contents: ALTERNATE 3V3 POWER
Size: B
DWG NO 510842-0001
Revision: C
Date: Monday, April 13, 2009
Sheet 52 of 53
VCC_3V3
BLM41P750SPT
L91
L92
C427 0.1uF
C431 10uF
C426 0.1uF
C430 10uF
TP68 TP-60
R508 15.8K
R509 30.1K
SPARE
TP67 TP-60
U42
TPS767D301
1RESET
1OUT_1
1OUT_2
1FB/SENSE
2RESET
2OUT_1
2OUT_2
2SENSE
THERMAL_PAD
1IN_1
1IN_2
1EN
1GND
2IN_1
2IN_2
2EN
2GND
NC.1
NC.2
NC.7
NC.8
NC.13
NC.14
NC.15
NC.16
NC.20
NC.21
NC.26
NC.27
C428 10uF
C429 10uF
VCC_5V
R510 10K
R511 NO-POP
TP69 TP-60
R504 10K
Q9
BSS138
R497 10K
R502 1K
TP70 TP-60
14.48.51 PWCTR_OUT1


SPECTRUM DIGITAL INCORPORATED
Title: DM365 Evaluation Module
Page Contents: POWER INPUT
Size: B
DWG NO 510842-0001
Revision: C
Date: Monday, April 13, 2009
Sheet 53 of 53
C15 47uF
VCC_5V
TP5 TP-30
R199 220
DS1 GREEN
D1 SMCJ6A
F1 F_4.0A
R199 NO-POP
CENTER SHUNT SLEEVE
J7 2.5 MM JACK RASM712
SILKSCREEN: 5V IN
TP40 TP-60
TP1 TP-60
TP2 TP-60
TP52 TP-60
TP51 TP-60
TP41 TP-60
GND Test Points

Appendix B

Mechanical Information

This appendix contains the mechanical information about the DM365 EVM produced by Spectrum Digital.


THIS DRAWING IS NOT TO SCALE
8.000
7.800
5.060
4.840
4.765
2.640
2.715
1.970
0.200
0.000
8.700
8.500
4.000
.125 DIA, TYP.
3.067
2.657
1.450
0.200
0.000
DM36X EVM
ASSY 510840 REV
VIDEO OUTPUTS
IMAGER INTERFACE
LCD INTERFACE
EMIF EXPANSION
ETHERNET
UART
EXIT
UP
MENU
SKIP -
SKIP +
LEFT
ENTER
RIGHT
REW
FF
KEY2
DOWN
KEY1
REC
STOP
PLAY
PAUSE

[redacted]

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